

First, here are generalized definitions of analog and digital signals and systems:

AN ANALOG SIGNAL IS ANY VARIABLE SIGNAL THAT IS CONTINUOUS IN BOTH TIME AND AMPLITUDE. IT DIFFERS FROM A DIGITAL SIGNAL IN THAT SMALL FLUCTUATIONS IN THE SIGNAL MAY BE MEANINGFUL.

A DIGITAL SYSTEM IS ONE THAT USES DISCRETE LEVELS OR NUMBERS, OFTEN BINARY, FOR INFORMATION REPRESENTATION, PROCESSING, TRANSMISSION, STORAGE OR DISPLAY RATHER THAN A CONTINUOUSLY VARIABLE ANALOG VALUE.



Figure 2 – Transition from analog to digital technology exemplified by mobile phones.

Electronics technology has a long history of transition between analog and digital approaches for system implementation. Generally, earlier systems are based on analog techniques which are then supplanted over time by digital designs. Perhaps the most obvious example is the computer. Early computers, in the 40s and even 50s were analog. When the digital computer became feasible, mostly due to the advent of component miniaturization and advancement in storage technology, the analog computer quickly became rare except for specialized applications. A similar thing occurred with audio reproduction technology. Analog records and magnetic tape were successful consumer technologies for decades until the advent of inexpensive CD and DVD technologies in the 80s and 90s. Now the digital approaches dominate over 95% of this market.

So why is power conversion still mostly in the analog domain?

The main reason is that efficiency is paramount in importance for most power system applications. No matter how many “bells and whistles” going digital might add, if it detracts from efficiency it will be a tough sell. The added power dissipation “overhead” in the form of additional circuitry for digital controls made this approach quite unattractive until very recently. Of course cost and packaging density are always issues as well. Happily, the recent advent of a mature CMOS digital technology has solved these issues by providing digital processing with high density, negligible power dissipation and low cost.

Power conversion is not the first application to take advantage of digital CMOS. A similar set of constraints (size, efficiency and cost) are also present in the markets for handheld battery powered communications devices such as transceivers and mobile phones. Both of these markets have transitioned to digital techniques in the past few years. Transceivers now use digital frequency synthesis rather than analog oscillators. Mobile phones now predominately use digital communications protocols rather than analog. Power conversion is now at the beginning of a similar transition to digital techniques based on CMOS circuitry.

2. POWER MANAGEMENT VS. POWER CONTROL

“Digital power” is a broad term that encompasses several concepts and sub-disciplines, and the end user can benefit from digital power on several different levels. This paper will identify and explain most of these concepts. One of the major themes of Ericsson’s approach to digital power is that for any given system application the end user will typically select only a subset of the possible digital power solutions that are available. This decision will be based on such factors as cost, complexity and system availability and maintenance requirements.

One key concept that must be understood is the distinction between power control and power management. Ericsson uses the term “power control” to address the control functions internal to a power converter, especially the cycle-by-cycle management of the energy flow within the converter. This will include the feedback loop and internal housekeeping functions. The power control function is “real-time” in comparison to the switching frequency of the power converter. These types of control functions can be implemented with either analog or digital techniques. Note that a converter could use digital power control techniques and appear identical to the end user to a similar converter using analog power control techniques. That is, the usage of digital power control may not require any changes or new design on the part of the end user.

Ericsson uses the term “power management” to address communication and/or control outside of one or more power modules. This would include such items as power system configuration, control and monitoring of individual converters, fault detection communication, etc. The power management functions are not real-time, because they operate on a time scale that is slower than the converter switching frequencies. Presently, these functions, when implemented, tend to be a combination of analog and digital. Output voltage programming of converters is often done with external resistors (analog). Power sequencing is typically done with dedicated control lines to each converter (digital). Digital power management, as defined by Ericsson, implies that all of these functions are implemented with digital techniques. Furthermore, rather than using multiple customized interconnections to each converter for sequencing and fault monitoring, some type of data communications bus structure is used to minimize the interconnection complexity.

2.1 POWER CONTROL

As explained above, power control relates to circuitry internal to a power converter, which can be thought of by the end user of a power module as at a device level. It is often possible for the end user to design successful power systems without knowledge of the internal implementation of the power converter, including its control system. Many users prefer to understand the internal operation of the converter in order to gain a better appreciation of its implementation and performance features. Ericsson discloses, at a block diagram level, the structure of its power modules so that this information can be available to its customers. In this section we will discuss, in a generalized way, how the converter control structures vary between analog and digital control and also identify some features that can be implemented using digital control that would not be practical in the analog realm.

On the right, *Figure 3* shows a classic analog converter control loop. A PWM IC is used as the primary control element. The converter output voltage is sampled by means of a resistive voltage divider and compared with a DC reference voltage by an error amplifier. The error amplifier output is an analog signal has a magnitude proportional to the needed correction in output voltage. This signal is used as an input to the PWM device, which produces an output pulse whose width is defined by the error signal. This PWM output pulse then is used to control the “on time” of the power handling semiconductors. MOSFETs are normally used as the power handling device. Their large input gate capacitance requires that driver circuits be used in order to turn them on and off in an efficient manner. For loop compensation, needed to insure the proper balance of dynamic response and stability, a fixed resistor capacitor network is typically used external to the PWM IC.

Two other major sections of the converter are the input and output filter networks. These sections, composed of inductors, capacitors and resistors, provide several functions. The input filter helps protect the converter from transients on the supply

voltage, provides some energy storage for converter operation during dynamic load changes, and includes filter networks to allow the converter to meet its input conducted emissions specifications. The output filter provides smoothing of the output voltage to insure that the ripple and noise specifications are achieved and also contains energy storage for servicing dynamic current requirements of the load circuits. It is important to note that the input and output filters and the power devices will remain essentially the same with either an analog or a digital control structure.

Below, *Figure 3* depicts the structure of a typical digital converter control system. The sensing of the output voltage is similar to that in an analog system. Rather than an error amplifier, however, the sensed analog voltage is converted to a binary digital number with an ADC. In addition to output voltage, it is useful to know the value of other analog parameters such as output current, temperatures in the converter, etc. Separate ADCs could be used for each parameter to be sensed, but it is often more advantageous to use just a single ADC and precede it with a MUX. The MUX will then sequence between the analog inputs to be measured and feed each one in sequence to the ADC.

The output of the ADC will be a series of digital numbers, each representing the value of a parameter at a specific time. Since the

clock frequency or sampling rate of the MUX and ADC is fixed, the result is a series of numbers for each parameter each separated by a known time period. The digital outputs from the ADC are fed to a μC which provides the processing for the system. On board ROM program memory is used to store the control algorithms for the μC . These algorithms allow the μC to perform a series of calculations on the digital outputs from the ADC. The results of these calculations are such parameters as the error signal, the desired pulse widths for the drivers, optimized values for delay in the various drive outputs, and also the loop compensation parameters. The external loop compensation components used with the analog approach are no longer needed.

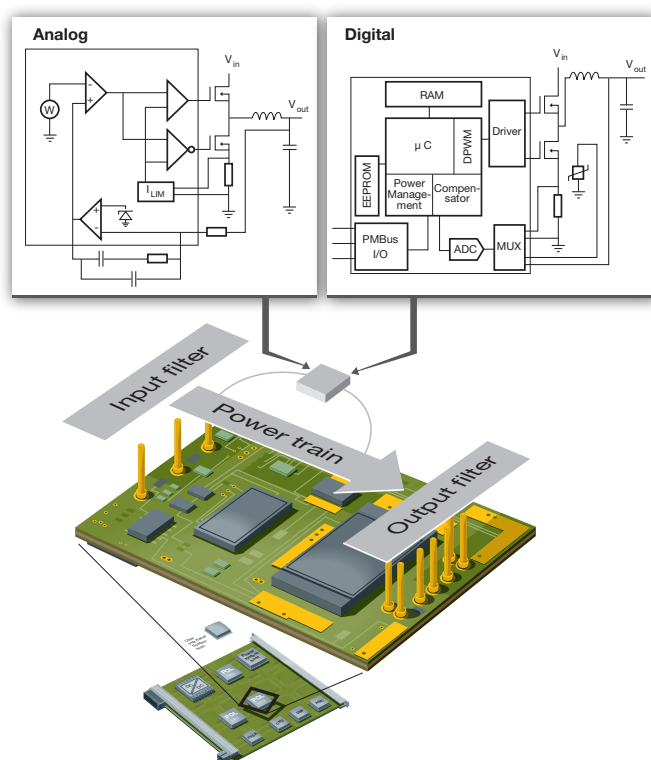


Figure 3 – Block diagrams of analog and digital control systems depicted together with some parts of the power train.

All values of parameters such as output voltage, output current and temperatures are stored in EEPROM at manufacturing or via transfer with the PMBus. The EEPROM content is down-loaded to the RAM during power-up and the μC is then using this part of the memory for read and write operations. The converter could be reset to default settings by an on-off sequence triggering a new EEPROM down-load. The optional use of the PMBus external to the converter will be discussed in detail later in this paper, but it is evident that this type of information about the converter operating parameters can be of considerable value to the overall system power management.

Digital control is considerably more flexible than analog control in its ability to adapt to changes in line and load conditions. Generally analog approaches are configured with only one “compromise” setting for a given control parameter whereas digital control systems have the ability to change the control parameters as a function of the converter operating conditions as illustrated by the following examples.

In a synchronous buck converter the top and bottom MOSFETs are operated so that both are never conducting simultaneously. This is guaranteed by defining a “dead time” period after one of them is turned off and before the other is turned on. When using an analog control system, the dead time is established by a fixed analog timing network, and the value of the dead time needs to be defined so that safe operation is guaranteed under the worst case combination of converter operating conditions. The downside is that under typical operating conditions the dead time is longer than required resulting in reduced converter efficiency. With digital control the dead time does not need to be fixed, but can be varied via a digital control loop as a function of operating conditions to optimize the converter efficiency (1). The efficiency algorithm actually measures the input and output energy delivery for a given dead time and then compares that result (efficiency) to another result with a slightly different delay time. The algorithm then adjusts the dead time either upward or downward to maximize the efficiency. The optimal value will change as a function of load current and other variables. This technique is especially valuable at low load as shown in the comparison in *Figure 4*. The plot shows that enabling the efficiency algorithm increases the efficiency at low load by several percentage points. The efficiency improvement is less at heavier loads, but extends over the entire operating range of the converter, more than compensating for any extra power overhead of the digital control circuitry.

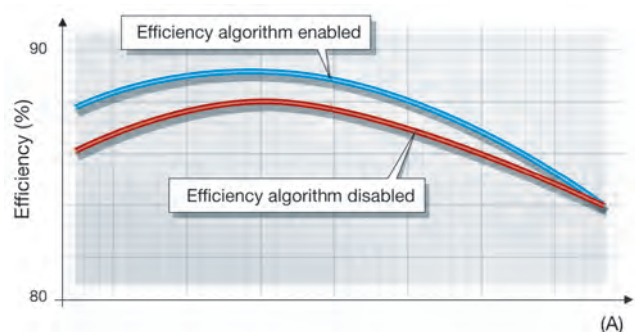


Figure 4 – A parameter such as “dead time” in a synchronous buck converter may be optimized over line- and load conditions to improve efficiency.

In analog control designs, the feedback loop compensation is a compromise between stability and dynamic response performance. Using digital control techniques it is possible to construct non-linear, or adaptive, control loops that change the compensation as a function of operating conditions. That is, the converter displays fast response when it needs to and slower response in other situations. *Figure 5* shows examples of this adaptive behavior. In addition to the enhanced dynamic response, this approach has other benefits to the power system. Fewer output decoupling capacitors will be required to insure a given voltage tolerance with resulting savings in cost and component space (2). Non-linear control can also be used to allow converter operation in discontinuous mode without the usual disadvantage of poor dynamic performance.

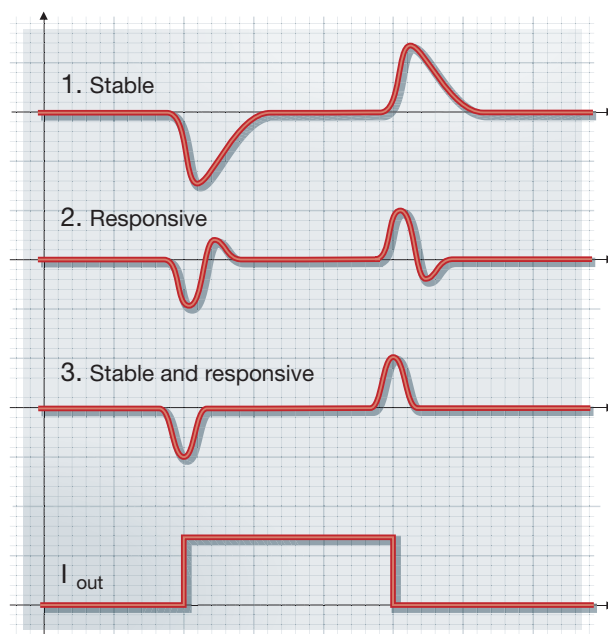


Figure 5 – Non-linear, or adaptive, control loops can combine the benefits of stability and responsiveness as exemplified by VOUT 3.

Multi-phase converters are a popular technique for generating high output currents with minimal output voltage ripple. However they become less efficient under light loading conditions due to the cumulative effects of switching losses from all the individual phases. Digital control can be used to operate with fewer phases at reduced current loads, a technique referred to as “phase dropping” (2). An example of the efficiency improvement with phase dropping is shown in *Figure 6*. At low load currents, the converter efficiency improves by several percentage points when dropping from 5 phases to 2 phases. This type of implementation and efficiency improvement is not practical with analog control.

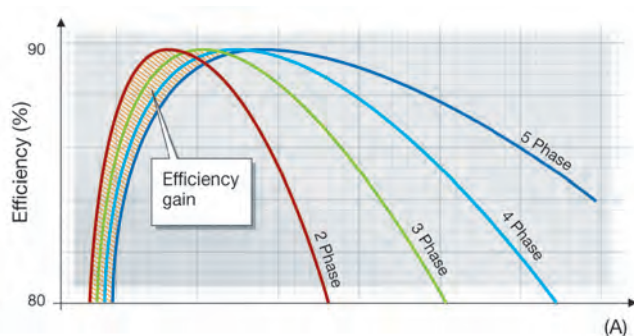


Figure 6 – A multi-phase converter may optimize efficiency by changing the number of phases used dependent on the output current.

Because of advantages such as those described above, Ericsson believes that digital control is now the preferred approach and will gradually be using more and more of it for new converter designs. We have seen that digital control inside the converter results in advantages to the system application such as improved efficiency, fewer external components and reduced cost. Even without any system power management considerations digital control is a clear winner. The fact that some of the embedded digital control circuitry in the converters can be used for system power management purposes is an added bonus. Thus much of the hardware for the power management capability that we will be describing in the next section comes “for free” as far as the system designer is concerned.

2.2 POWER MANAGEMENT

We will now explore how digital power management can benefit power systems at all stages of their design, manufacture and deployment. We will see that flexibility is the key and that the power system designer may pick and choose only those features and capabilities that he/she feels are important to a specific application.

The digital power management systems and features to be described here assume a basic architecture consisting of power converters that communicate with some sort of centralized control device via a digital communications bus. The converters can be either isolated DC/DC converters or non-isolated point-of-load converters. The centralized control device can also take many forms, including:

- AN IC DEDICATED FOR POWER SYSTEM CONTROL
- A GENERAL PURPOSE MICROCONTROLLER
- SPARE GATES IN A SYSTEM FPGA
- A LAPTOP COMPUTER WITH A GUI
- ATE DURING THE CONVERTER OR SYSTEM TESTING PROCESS

This general architecture is referred to by various terms. The centralized control element is often called the “host” or the “master” or the “controller”. The controlled converters are referred to as “slaves” or sometimes just as “devices” or “power supplies”. Unless otherwise stated, the discussion here assumes that the host device has a control domain consisting of a single system board. This will be the actual case for many if not most power systems. For some larger scale systems, this host will in turn interact with higher level controllers elsewhere in the system or perhaps even with remotely located devices via long distance communications networks. *Figure 7* is a depiction of the generalized control architecture that will be the basis for the following discussion.

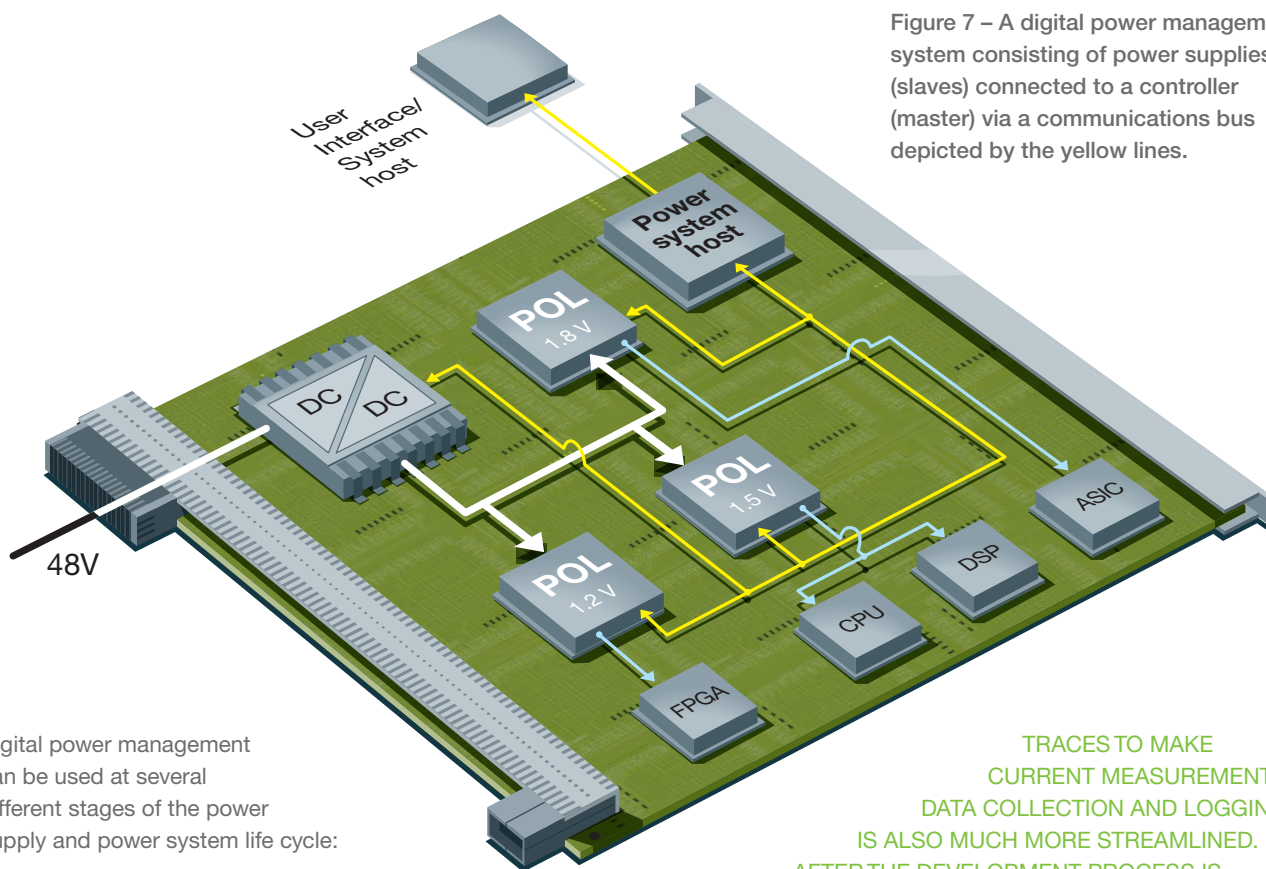


Figure 7 – A digital power management system consisting of power supplies (slaves) connected to a controller (master) via a communications bus depicted by the yellow lines.

Digital power management can be used at several different stages of the power supply and power system life cycle:

- DURING MANUFACTURING OF THE POWER SUPPLY, ATE CONTROL CAN BE USED TO CONFIGURE POWER SUPPLY PARAMETERS SUCH AS OUTPUT VOLTAGE TRIMMING, TRIP POINTS FOR OCP / OVP / OTP, AND LOADING OF DATE CODES AND SERIAL NUMBERS. IN ADDITION TO USING THIS APPROACH FOR STANDARD CONVERTERS, ERICSSON CAN CUSTOMIZE CONVERTERS FOR SPECIFIC CUSTOMERS. FOR EXAMPLE, VOUT SET TO 3.4V, OVP TO 3.9V AND OCP AT 13 A. THE CUSTOMER CAN THEN USE THIS CONVERTER WITHOUT ANY DIGITAL POWER MANAGEMENT – I.E. THE SAME AS AN “ANALOG” CONVERTER.
- DURING OPTIMIZATION OF THE POWER SYSTEM DESIGN, THE OEM ENGINEER CAN UTILIZE THE DIGITAL INTERFACE TO THE POWER CONVERTERS BY CONNECTING THE COMMUNICATIONS BUS TO A LAPTOP COMPUTER AND GUI TO EASILY MEASURE TEMPERATURE, VOLTAGES AND OUTPUT CURRENTS, TO SET THE TRIP POINTS FOR FAULT PROTECTION CIRCUITS AND TO OPTIMIZE THE POWER SEQUENCING. THIS WILL BE A MUCH EASIER AND FASTER PROCESS THAN THE CONVENTIONAL APPROACH WITH ANALOG CONTROLS THAT INVOLVES INSTALLING SEVERAL ITERATIONS OF CONTROL COMPONENTS AND HACKING INTO PC BOARD
- TRACES TO MAKE CURRENT MEASUREMENTS. DATA COLLECTION AND LOGGING IS ALSO MUCH MORE STREAMLINED. AFTER THE DEVELOPMENT PROCESS IS COMPLETE, THE DESIGNER CAN REMOVE THE DIGITAL INTERFACES IF DESIRED BEFORE THE PRODUCT GOES INTO PRODUCTION.
- DURING PRODUCTION ASSEMBLY AND TESTING OF THE BOARD AND SYSTEM THE DIGITAL POWER MANAGEMENT INTERFACE CAN BE USED BY ATE FOR SUCH PURPOSES AS VOLTAGE MARGIN TESTING, VOLTAGE MONITORING AND TRIMMING, MEASURING CONVERSION EFFICIENCY AND RECORDING SERIAL NUMBERS AND DATE CODES FOR SUPPORT TRACEABILITY.
- IF THE SYSTEM DESIGNER PLACES A PERMANENT HOST CONTROLLER ON THE BOARD FOR USAGE DURING NORMAL OPERATION, THEN A WHOLE WORLD OF OPPORTUNITIES IS CREATED. SOPHISTICATED START-UP AND SHUT-DOWN SEQUENCING CAN BE PROVIDED WITHOUT THE COMPLEXITY OF ADDED COMPONENTS AND INTERCONNECTIONS. OPERATING TEMPERATURES CAN BE EASILY MONITORED FOR PURPOSES OF REGULATING SYSTEM FAN SPEEDS. EFFICIENCY MAY BE MONITORED IN REAL TIME AND DEGRADATION NOTICED BEFORE ACTUAL FAILURES OCCUR. FAULT DETECTION AND MANAGEMENT ROUTINES CAN BE DEVELOPED THAT TAKE INTO ACCOUNT CONDITIONS ELSEWHERE IN THE SYSTEM.

While the usage of digital power management at various stages of the system is optional and not required, it does offer several benefits and opportunities. Space does not permit discussing all of them, but below are some examples which are grouped under the categories of control, configuration and monitoring.

System power control is becoming more complex as the number of voltage levels on a typical board is increasing. The additional levels greatly increase the complexity of the voltage sequencing. Sequencing order, ramp times and delays need to be controlled for both normal start-up and shut down operation as well as for some fault conditions. All this is quite easy to accomplish with digital management without resort to installing analog control and timing components or even using a soldering iron. Event-driven sequencing can also be easily configured – for example verifying the performance parameters of converter #1 before turning on converter #2.

Voltage margining is another example of using digital management for converter control. This is used during the final stages of production for “corner testing” in order to verify the robustness of the unit. Voltages are varied by perhaps +/- 5% in different combinations. Using the digital communications bus, this can be accomplished in less than a second without any additional hardware or interconnections. *Figures 8 and 9* show examples of both sequencing and margining.

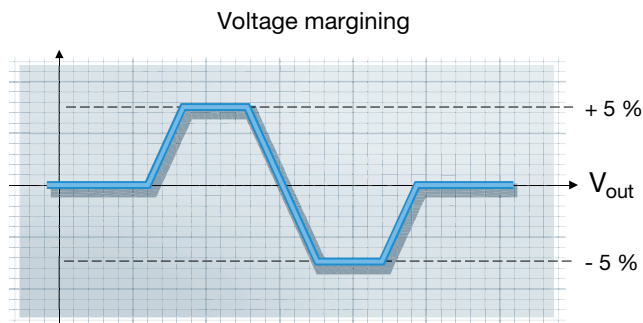


Figure 8 – Digital power management may be used for voltage margining of the output from the converter (corner testing).

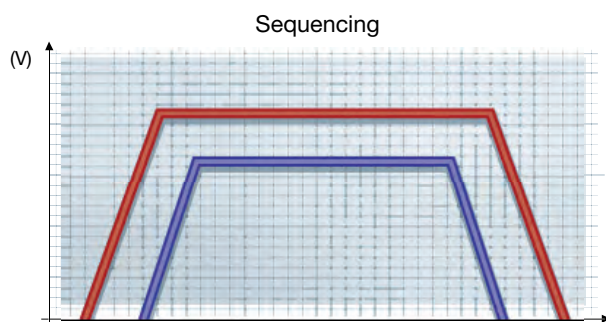


Figure 9 – The sequencing order for start-up and shut-down of multiple converters may be controlled using digital power management.

A common requirement that falls into the configuration category is programming thresholds for fault detectors. Using a digital bus results in extreme flexibility in this regard:

- OTP CAN BE SET CONVENTIONALLY TO A FIXED VALUE DEPENDENT UPON THE MAXIMUM ALLOWED BY THE POWER CONVERTER. SOME USERS MAY WANT TO SET IT TO A DECREASED VALUE EITHER TO REDUCE THE LOCALIZED HEAT LOAD AROUND SENSITIVE COMPONENTS NEAR THE CONVERTER OR TO ENHANCE SYSTEM RELIABILITY. THE OPERATION OF THE OTP CAN ALSO BE CONFIGURED DIGITALLY FOR EITHER LATCHING OR AUTOMATIC RESTART.
- THE OCP TRIP POINT CAN BE SET CONVENTIONALLY TO A FIXED VALUE DEPENDENT UPON THE CONVERTER'S MAXIMUM OPERATING CURRENT. THE TRIP POINT CAN BE REDUCED VIA THE DIGITAL BUS IF A LOWER MAXIMUM CURRENT IS DESIRED TO PROTECT THE LOAD CIRCUITRY OR DISTRIBUTION TRACES. LATCHING OR AUTOMATIC RECOVERY MODES CAN BE PROGRAMMED. THE NUMBER OF RETRIES FOR “HICCUP” MODE RESTART CAN BE PROGRAMMED. THE OCP CAN EVEN BE PROGRAMMED TO BE TIME-VARIANT. FOR EXAMPLE, IF A LOAD HAS A KNOWN SURGE CURRENT FOLLOWED BY A LOWER OPERATING CURRENT, DIFFERENT OCP TRIP LIMITS CAN BE USED DURING THESE TIME PERIODS.
- THERE IS ALSO EXTREME FLEXIBILITY IN THE CONFIGURATION OF OVP. THE OVP TRIP POINT CAN BE PROGRAMMED TO DIFFERENT VALUES AS THE OUTPUT VOLTAGE IS TRIMMED SO THAT OVP PROTECTION IS PROVIDED WITHOUT NUISANCE TRIPPING. BOTH LATCHING AND AUTOMATIC RECOVERY MODES ARE AVAILABLE AND EASILY PROGRAMMED.

It is important to note that the usage of digital configuration does not necessarily require the inclusion of a host controller or digital bus in the user's end system or even in the system manufacturing process. If the configuration requirements are known and will remain relatively fixed, Ericsson can easily program them into the converters during the power module manufacturing process without any hardware changes. The OEM customer can then use the power module the same way he would a conventional analog module.

An interesting example of digital configuration is to facilitate second-sourcing of power converters. While it is fairly easy to locate second sources that have the same volts and amps on the output, there are quite often differences between manufacturers in terms of the fault protection implementation. For example, you have designed around source A which has a start-up ramp of 30 ms and latching OCP. You find source B which is similar except that the start-up ramp is 10 ms and the OCP has automatic recovery. Making these kinds of changes to

source B in an analog domain is very complex and expensive, requiring new part numbers, new components, new PCB layouts in some cases and a lengthy development time. With digital configuration, these changes can be programmed into a converter without any impact to the hardware, cost or development time.

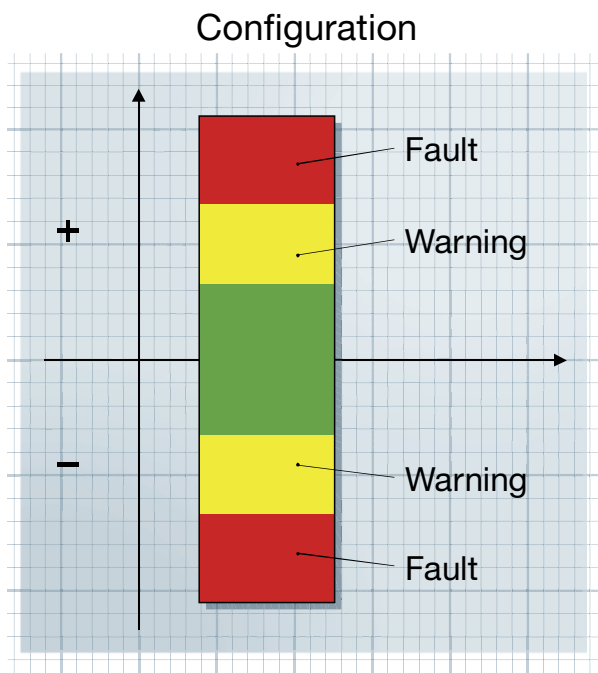


Figure 10 – Limits for both warning and fault conditions may be programmed for parameters such as temperature, output voltage and output current.

Monitoring consists of measurement of such parameters as input and output voltages and currents, operating frequency, and temperatures interior to the power converters. Most OEMs will find this capability to be of the greatest use during the design and evaluation phases of a new system. Digital

monitoring allows for all of these measurements to be made via a laptop computer and GUI rather than with thermocouples, soldering irons and component replacements. Gaining parametric information at this stage allows for optimization of the power system and for the selection of the most cost-effective power converters.

Designers of high end and high availability systems may want to extend these kinds of capabilities into the final product itself so that parametric data may be collected in the system operating environment. This will, of course, necessitate the inclusion of some kind of host controller within the product and possibly communication outside of the system to a higher level data management system. An infrastructure must also be in place to handle the collected data. Some examples of the kinds of capabilities possible with this type of approach are:

- EFFICIENCY MAY BE MONITORED DURING FIELD OPERATION AND DEGRADATION NOTED PRIOR TO ACTUAL FAILURE SO THAT PART REPLACEMENTS CAN BE MADE WITHOUT AFFECTING SYSTEM AVAILABILITY.
- SYSTEM FAN SPEED CAN BE CONTROLLED AS A FUNCTION OF ACTUAL TEMPERATURES INSIDE OF POWER CONVERTERS.
- A COMPLETE FIELD POPULATION OF SYSTEMS COULD BE QUERIED TO FIND THE LOCATIONS OF POWER CONVERTERS WITH A PARTICULAR SERIAL NUMBER RANGE OR DATE CODE FOR THE PURPOSE OF REPLACING A SUSPECT BATCH OF CONVERTERS BEFORE THE ADVENT OF FIELD FAILURES.

Most users will not need to use this degree of sophistication in their designs. An approach intermediate in complexity is to use an interrupt-driven design in which the host controller does not do routine monitoring of parametric data, but is only notified by a power converter when it is experiencing a problem. The host can then take the required action as a function of the converter fault mode.

3. PMBUS

Ericsson has selected the PMBus as the interface for digital power control and management of its applicable products. The PMBus is not an Ericsson development, but rather an existing protocol that has been adopted and supported by Ericsson as well as by several other power supply manufacturers. The protocol is owned by the System Management Interface Forum (SM-IF). Membership in SM-IF is open to all interested parties, and the PMBus specification is freely distributed and is available for usage on a royalty-free basis. The bus will be described briefly in this paper so that the reader can understand how it contributes to the concept of digital power. We will not go into extensive detail, however, since the latest complete information is easily available from the PMBus (3) and SM-IF (4) websites.

The PMBus is a broad, generic and flexible interface that can be applied to a wide range of devices. It works well with all kinds of power products including isolated DC/DC converters, non-isolated POL converters, bus converters, AC/DC converters as well as fans. The PMBus is not a product in itself and it is also not a standard for power supplies or for DC/DC converters. The bus definition does not extend to the point of establishing form factors, pinouts, and complete structural details of the interconnection components. Alliances such as POLA and DOSA will define the actual implementation for many suppliers. The PMBus addresses the host to controlled device communication architecture described earlier and does not include provision for direct device to device communication.

Facts about PMBus

Open communication standard
to **Configure**
Control
Monitor all types of power
converters

Royalty Free and Freely available
specifications

Owned by:
System Management
Interface Forum (SM-IF)

Supported By:

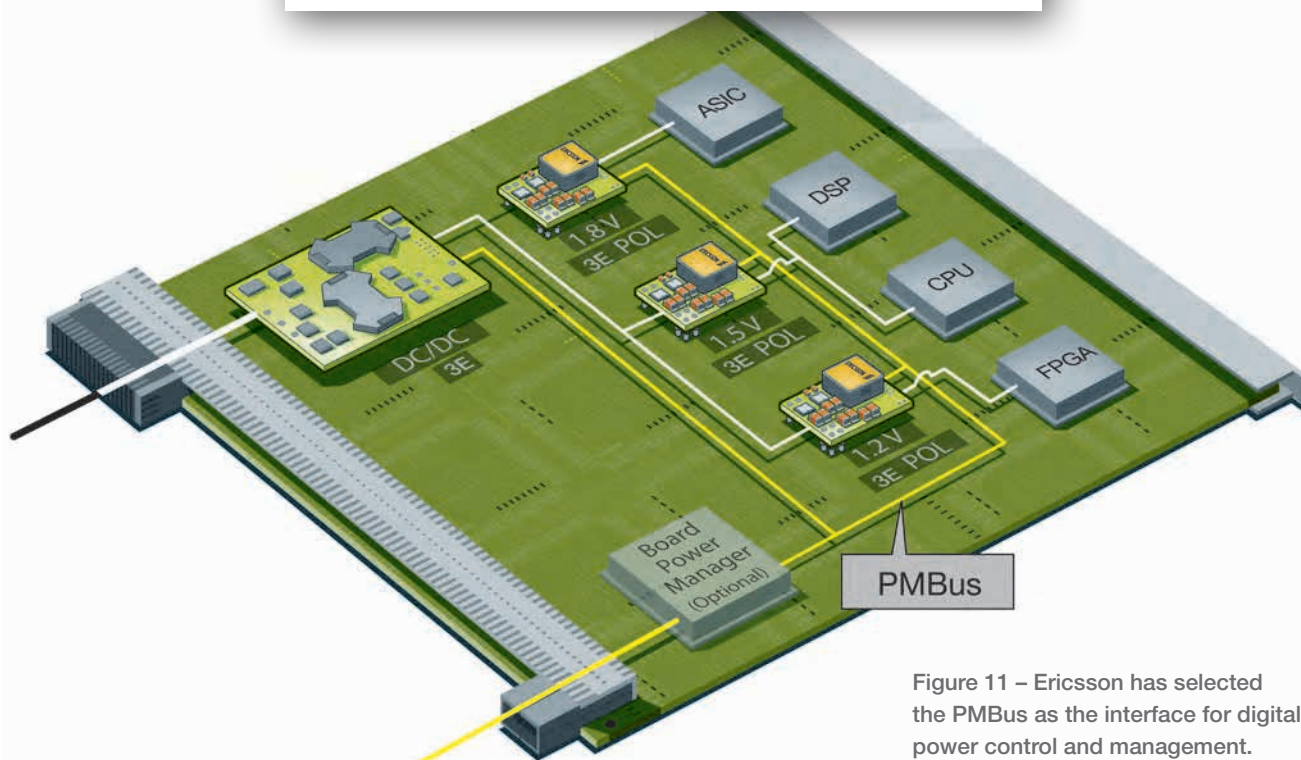


Figure 11 – Ericsson has selected the PMBus as the interface for digital power control and management.

Consequently, it will not directly support converter to converter interaction such as is sometimes used for current sharing or analog voltage tracking implementations. These kinds of capability will continue to exist, but they will be implemented by other methods developed by IC and power supply manufacturers. The intent is to provide a dependable and widely used and understood digital power control and management interface without limiting innovation of other advanced techniques.

The PMBus protocol is defined in a layered manner, and basically defines the rules for sending blocks of data from node to node in the network. The physical layer defines the fundamental interconnection. In its most basic form, the PMBus is a two wire serial bus that is based upon the SMBus, which is a derivative of the popular I2C bus originally developed by Philips, but enhanced to provide greater functionality for power control applications. The command language layer defines the commands, data formats and information handling.

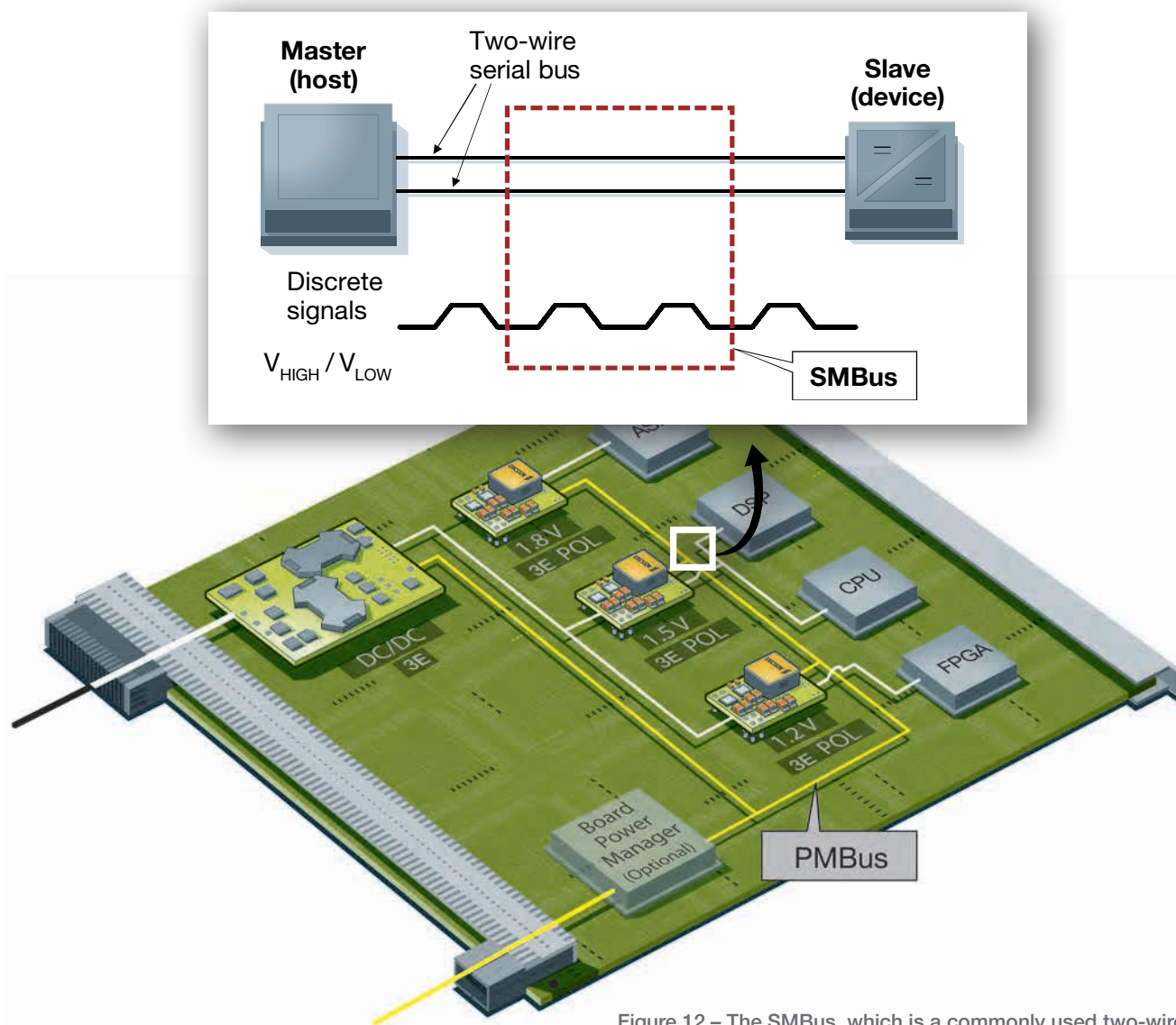


Figure 12 – The SMBus, which is a commonly used two-wire serial bus, forms the foundation for data transportation on the PMBus.

Every implementation of the PMBus will have two main signals or lines which are called DATA and CLOCK connecting the host with each controlled device. In addition to these two required signals, there are optional extensions to the PMBus. A line called CONTROL can extend from the host to one or more controlled devices. The CONTROL line is used to define on and off conditions for controlled devices in a manner similar to the Remote Control and Inhibit signals that are commonly used with present power converters. Another optional signal is called SMBALERT#. This signal is essentially an interrupt that goes from a controlled device to the host for notification of a

problem or situation that needs attention from the host. There is also an option on the controlled devices for WRITE PROTECTION. WRITE PROTECTION is a single connection or pin that prevents data stored in the controlled device from being overwritten by the host. A summary of these signals is shown in *Figures 13 and 14*. The data flow direction is depicted by the arrowheads in the drawing. Configure and Control commands flow from the host to the controlled devices. Monitoring information flows from the controlled devices to the host. Both of these information transfers occur by using the DATA and CLOCK lines under control of the host.

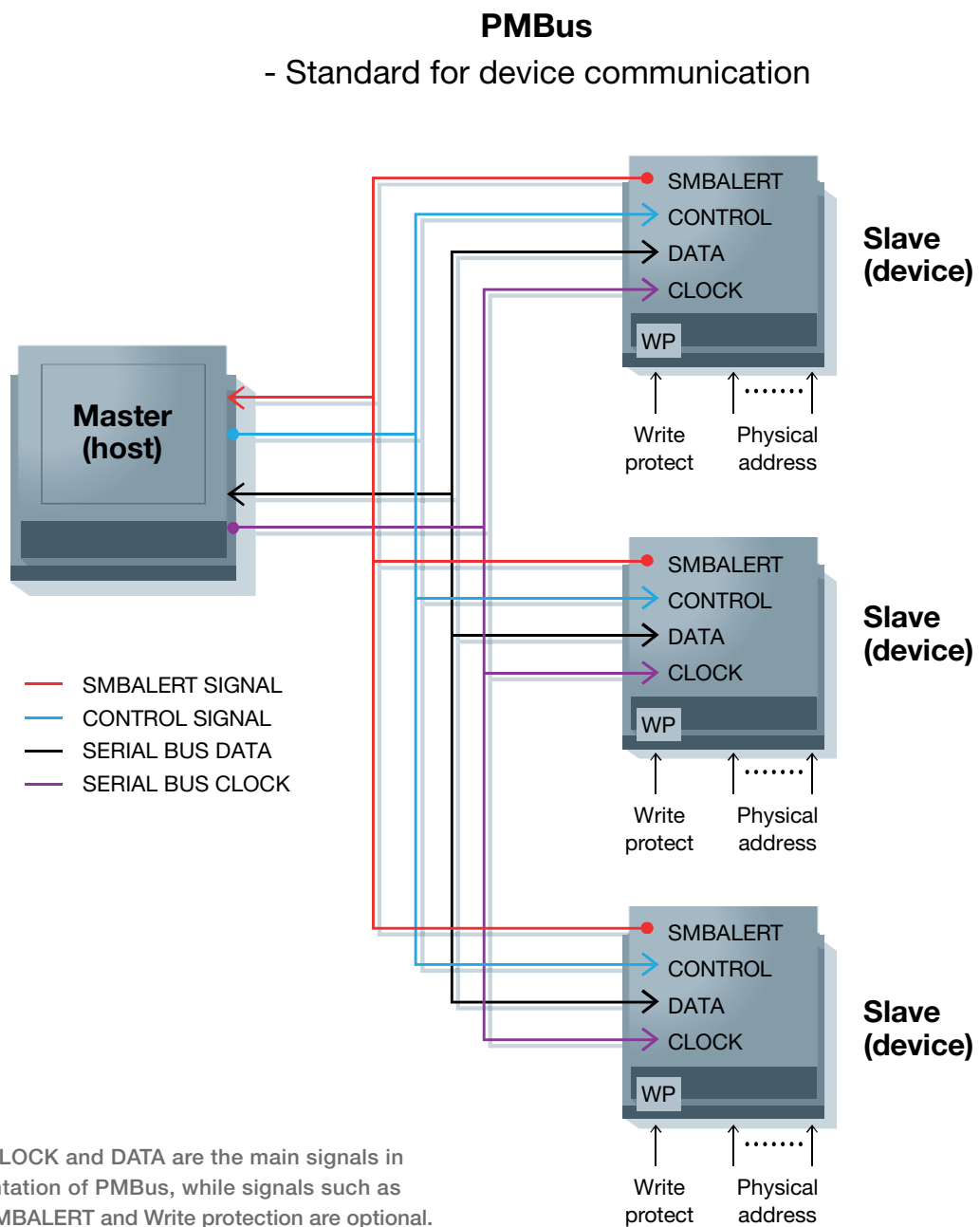


Figure 13 – CLOCK and DATA are the main signals in the implementation of PMBus, while signals such as CONTROL, SMBALERT and Write protection are optional.

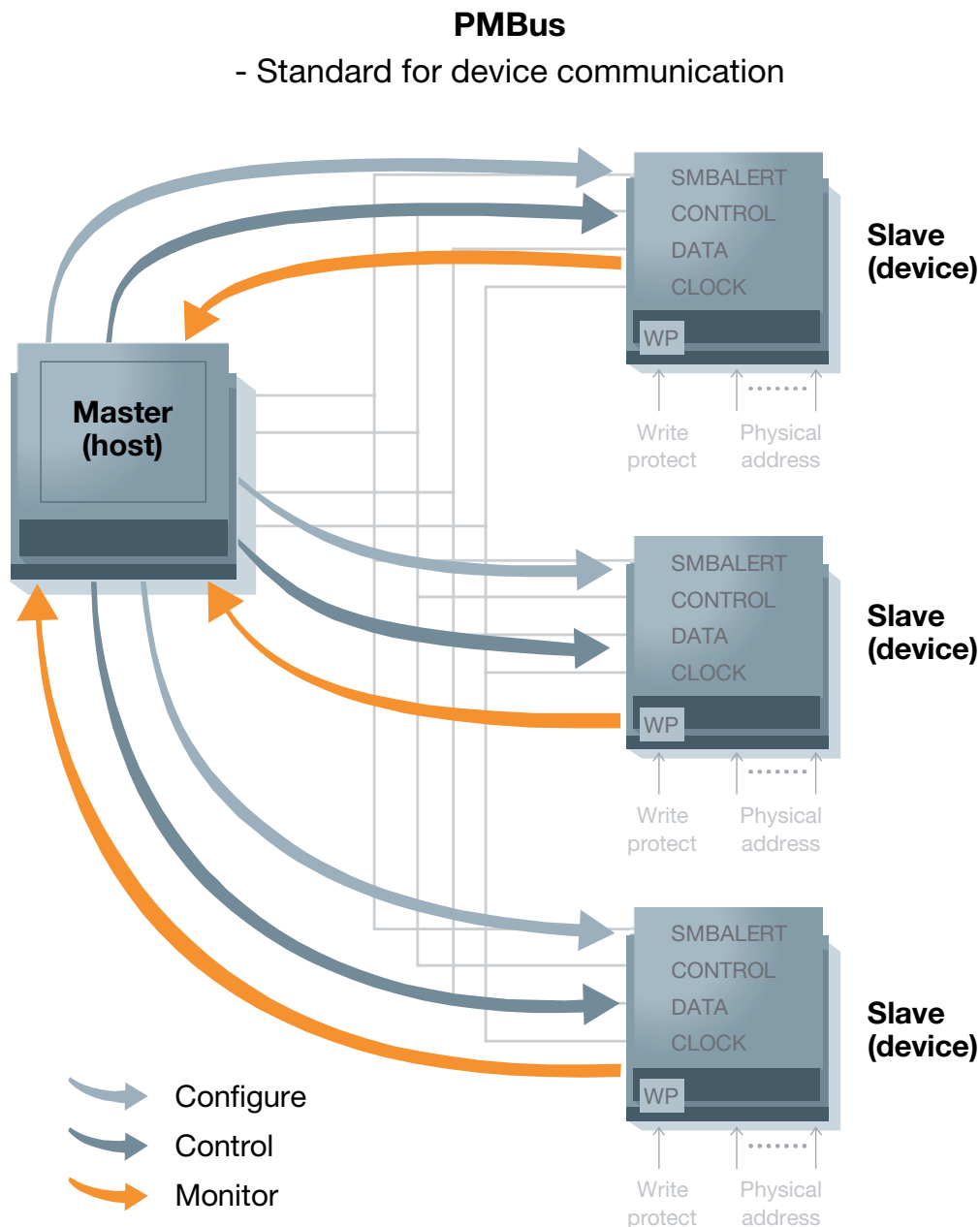


Figure 14 – Configure and Control commands flow from the host to the controlled devices. Monitoring information flows from the controlled devices to the host.

Each controlled device must have a unique 7 bit physical address to be compliant with the PMBus protocol. While PMBus requires a 7 bit physical address for each controlled device, it does not specify how these addresses are established. This is because there are several methods for accomplishing the addressing and flexibility is important, allowing different hardware suppliers to use different address assignment methods and yet still be compatible with the PMBus.

The physical address is similar to a phone number in a telecom system or an IP address in a TCP/IP system. It is a unique identifier which allows the host to know which device it is communicating with. The 7 bit addressing will allow for over a hundred unique addresses which are more than enough for most any power system application. The switching speed limitation due to capacitance in the physical bus would most likely form a constraint if such a larger number of devices are connected to a single controller node.

One way of establishing a physical address in a controlled device is to use binary pin programming. Each programming pin can be tied to ground for one logic state or left open for the other. For example, with 5 programming pins, there are 25 or 32 possible physical addresses. Five extra pins on many power converters represent a significant penalty in terms of cost and size while still having a fairly limited number of possible addresses. Another approach is to use tri-state output drivers on the pins. This gives three states (high, low, open) on each pin and increases the addressing density somewhat. For example, with 3 pins, there would be 33 or 27 possible addresses. There can be power sequencing problems with the tri-state approach however. The internal voltage required to define the “high” state might not be available until after the converter is powered up.

One approach that seems promising to Ericsson is to use a resistor trim technique and only a small number of pins. Multiple states can be defined on a single pin by connecting a constant current source internal to the converter to ground through an external programming resistor. Predefined resistor values would correspond to different voltage levels across the resistor which in turn would correlate with a digital level. For example if a 10 mA current source is used in conjunction with 25 kW resistor steps, voltage steps of 0.25 V will result. Eight of these voltage steps would scale from 0 to 2 V. Using only two of these pins would allow for a total of 82 or 64 unique physical addresses.

The jury is still out on what will be the most popular addressing techniques. In any event, the preferred solution should be a good balance between the following considerations:

- THE NUMBER OF CONNECTION PINS SHOULD BE SMALL TO REDUCE SIZE AND COST.
- ENOUGH UNIQUE ADDRESSES SHOULD BE AVAILABLE FOR ANY PRACTICAL POWER SYSTEM.
- THE TECHNIQUE MUST BE ROBUST AND STABLE WITHOUT ANY UNINTENDED STATE CHANGES DUE TO NOISE.

As mentioned earlier, the actual physical implementation is not defined by the PMBus. In the case of Ericsson's power products, we are cooperating with both DOSA and POLA for the purpose of establishing standard configurations for form factors, pinouts and mechanical interfaces for the PMBus connections and programming pins.

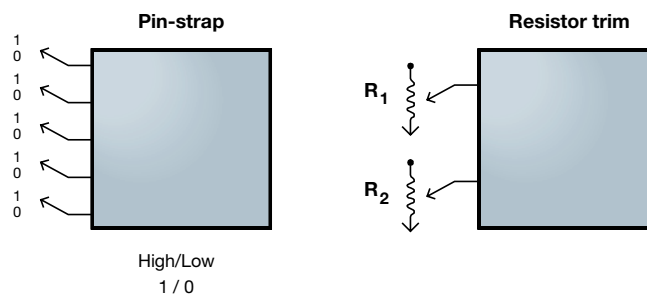


Figure 15 – Unique addresses can be assigned by means of different techniques like pin-strap or resistor trim.

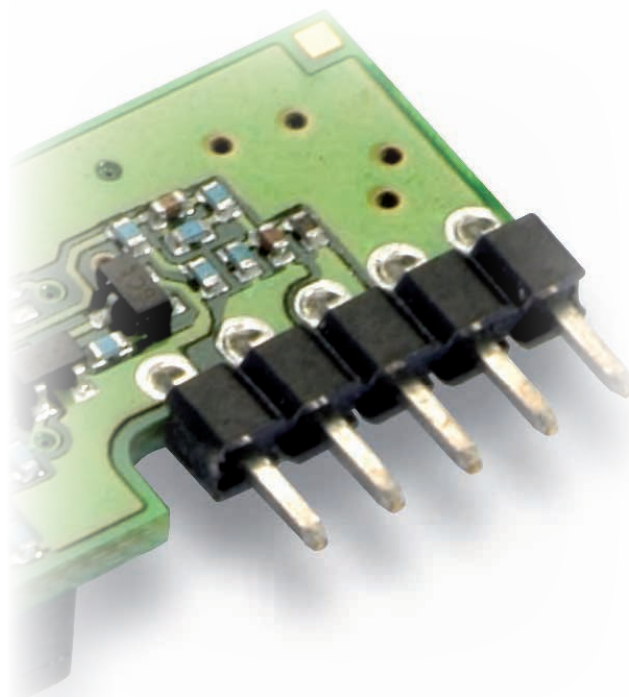


Figure 16 – Pinouts and mechanical interfaces are not defined in PMBus. Ericsson will be instrumental in defining those by cooperating within both DOSA and POLA.

4. DIGITAL TECHNOLOGY FEASIBILITY

For many decades analog techniques have been successfully used to manufacture power converters. The most recent analog designs are most remarkable, exhibiting extremely high efficiency, high packaging density, fast dynamic response, excellent reliability and reasonable cost. While digital power techniques have been proposed for some years now, they would not have been able to successfully compete with analog solutions. Digital signal processing would have resulted in more cost, less efficiency due to power dissipated for control circuitry, slower performance and larger size.

We are now at a fortuitous time in technology development where the right pieces are in place to swing the balance in favor of digital control approaches. Thanks to Moore's law and the corresponding

increase in IC density, hard work on the part of semiconductor suppliers and a mature and reliable CMOS technology, digital processing for power conversion applications now is very attractive. While leading edge CMOS geometries are now in the 65 to 90 nm linewidth region, the best approach for power conversion is to use the less expensive but very proven geometries in the range of 0.18 to 0.35 μm . These devices are manufactured in enormous volumes with very high yields and very reasonable costs and have the required speed and performance for power conversion applications. More importantly, the use of digital techniques results in capabilities and performance levels at both the converter and system levels that are not possible with analog. *Figure 17* shows how the cost and performance tradeoffs have changed over time for analog and digital approaches to power conversion control.

The technology evolution

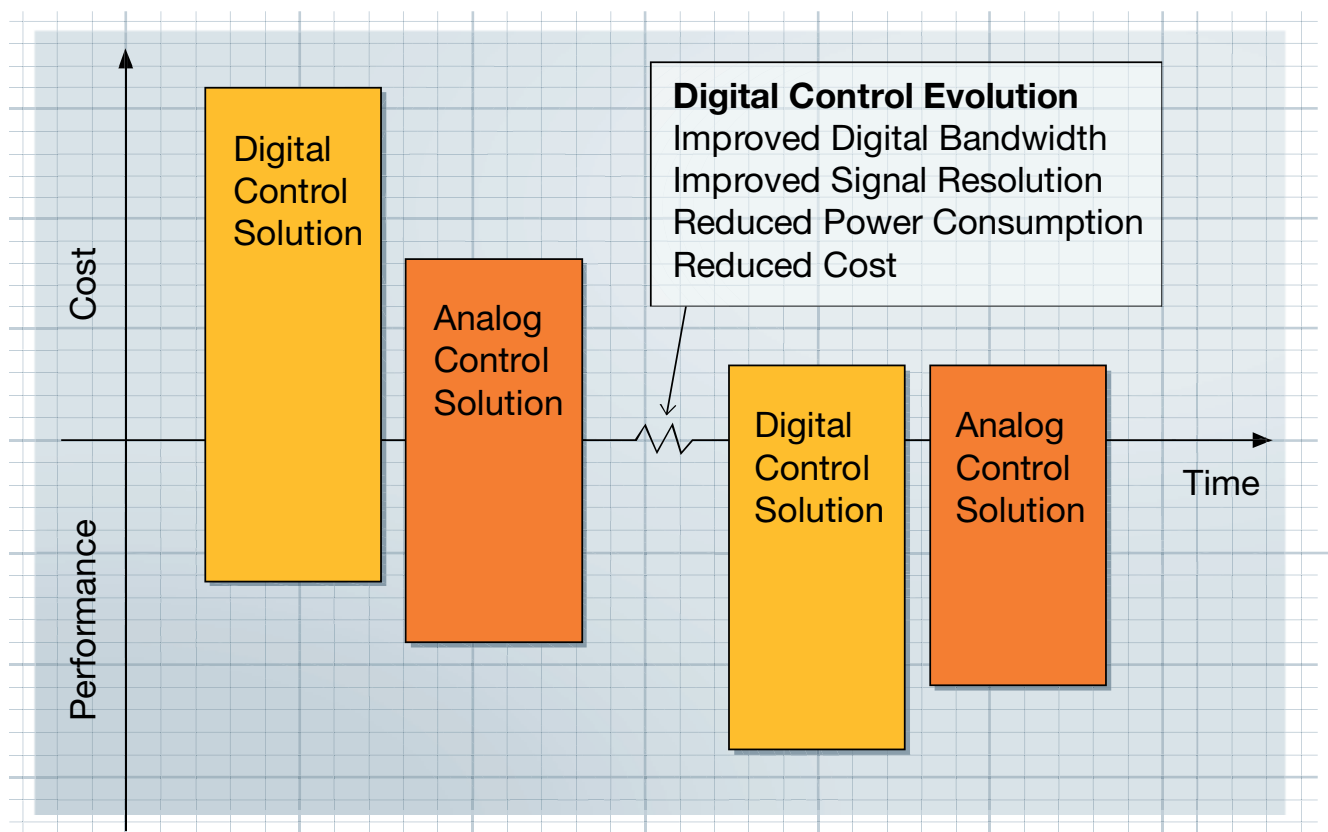


Figure 17 – Mature and reliable CMOS technology is about to swing the balance in favor of digital control approaches.

5. CUSTOMER VALUE

5.1 ADVANTAGES OF DIGITAL CONTROL AT POWER CONVERTER LEVEL

While much of the publicity and controversy about digital power techniques is focused on power system management issues, Ericsson feels that the most important issue, and the ultimate driver for its acceptance, will be the benefits that it brings to the power converter itself. These benefits are real, measurable and available with today's technology. In this section we will summarize how digital control approaches affect the performance of power converters in an "apples-to-apples" comparison with present day analog technology. These benefits will be available to users of the digitally controlled converter even if there is no digital power management undertaken at the system level. In other words, the converter could be considered as an "improved analog" design if the user is uncomfortable with using digital terminology.

- **IMPROVED EFFICIENCY DUE TO OPTIMIZATION OF SEMICONDUCTOR DEAD TIME AND PHASE DROPPING IN MULTI-PHASE CONVERTERS. RESISTIVE LOSSES ARE ALSO REDUCED BECAUSE THE SMALLER FOOTPRINT OF DIGITAL CONTROL CIRCUITRY FREES UP MORE AREA FOR COPPER TRACES.**
- **IMPROVED RELIABILITY DUE TO HIGHER INTEGRATION OF DIGITAL CONTROL CIRCUITRY AND FEWER OVERALL CONTROL COMPONENTS.**
- **FEWER EXTERNAL DECOUPLING CAPACITORS DUE TO ENHANCED LOAD TRANSIENT RESPONSE OF ADAPTIVE DIGITAL CONTROL. THIS WILL REDUCE SYSTEM COST.**
- **INCREASED CONVERTER POWER DENSITY POSSIBLE DUE TO SMALLER DIGITAL CONTROL CIRCUITRY. THIS CAN RESULT IN EITHER INCREASED POWER OR SMALLER CONVERTERS.**
- **TIGHTER OUTPUT VOLTAGE TOLERANCES DUE TO ENHANCED INITIAL SET POINT TRIMMING CAPABILITY AND MORE SOPHISTICATED TEMPERATURE COMPENSATION ALGORITHMS.**
- **LOWER OVERALL COST OF OWNERSHIP DUE TO ABOVE EFFICIENCY, RELIABILITY AND COMPONENT REDUCTION IMPROVEMENTS**

As described above, there are several tangible benefits to digital control that are available to all users of these converters. Due to the cost parity between digital and analog control implementations using today's technology, these benefits are "free" to the end user and represent real customer value. Additional benefits at the system level are available if the user elects to implement some of the optional digital power management techniques described in the next section.

5.2 ADVANTAGES OF DIGITAL MANAGEMENT AT SYSTEM LEVEL

There are sound advantages in utilizing the digital interface to power converters during the system design, development and evaluation periods. The communications bus allows for complete user customization of many converter parameters while the converter is actually in the prototype system. Performance monitoring is also considerably easier and faster. The net result is a reduction in design time, facilitated power management and a resulting reduction in time-to-market for the end product. Technical risk is also considerably reduced because the configurability capability of the digital communications bus will allow for optimization and tweaking of the selected power converter rather than having to substitute alternative physical converters, perhaps from different suppliers, as the development process proceeds.

In fact, the digital communications bus can be used to essentially create second source power converters in many cases by configuring the power converter's fault handling implementation to match that of the converter being replaced. The configurability also allows a single converter part number to serve several purposes, thereby reducing the number of part numbers being managed, the inventory, and the time required for sourcing converters. Note that none of these capabilities will require any changes in hardware. These types of advantages may be applied at both the OEM site and at the power converter manufacturing site, resulting in expected lower parts management costs and faster delivery times.

The reduction in technical risk and improvement in time-to-market also extends into the design of the power management system itself. With an analog based control structure, the typical solution is a fully custom mixed-signal control design consisting of dozens of analog components, one or more power management ICs and perhaps analog to digital conversion to a non-standard digital interface. This approach requires extensive design time and tends to have limited flexibility in terms of accommodating future changes in power system requirements. If the PMBus management approach is adopted from the beginning, the system power management hardware tends to be much more standardized and not require much in the way of custom design. The PMBus is also very extendable so that future changes or additions to the power system may be easily accommodated. Due to the large number of voltage levels in today's power system designs and the expected further increase in multiple core voltage levels, this improved and lower risk power management capability is a very important consideration.

The major benefits to the user are:

- A TAILOR-MADE OR SEMI-CUSTOM CONVERTER MAY BE QUICKLY CONFIGURED EITHER BY THE CONVERTER MANUFACTURER OR AT THE OEM SITE
- SOFTWARE BASED DESIGN CHANGES WILL STREAMLINE THE PARTS SUPPLY PIPELINE AND REDUCE COSTS
- RISK AND TIME-TO-MARKET WILL BE IMPROVED

It is worth stating again that some of these benefits can be attained without using the PMBus in the final shipped product. Using digital management and monitoring only during the engineering development period and perhaps during manufacturing testing will provide significant benefit while reducing risk and time-to-market.

The ultimate extension of the PMBus digital power management concept is to use it in the end product in the field environment for purposes of power system control, monitoring, supervision and fault handling. Some of the possible implementations of this concept include:

- USING THE PMBUS ONLY FOR POWER ON/OFF SEQUENCING AND HIGH LEVEL FAULT HANDLING WITHOUT REAL-TIME MONITORING OF OPERATING PARAMETERS.
- MONITORING OF CONVERTER OPERATING TEMPERATURES WITH FEEDBACK TO SYSTEM FAN SPEED CONTROLS.
- REAL-TIME MONITORING OF CONVERTER OPERATING EFFICIENCIES AND FAULT ANTICIPATION ALGORITHMS BASED UPON SENSING EFFICIENCY DEGRADATION.
- SOPHISTICATED SYSTEM LEVEL FAULT HANDLING ROUTINES BASED UPON MONITORED CONVERTER DATA.
- IDENTIFICATION OF LOCATION OF SPECIFIC SERIAL NUMBERS OR DATE CODES IN A LARGE FIELD POPULATION OF CONVERTERS FOR THE PURPOSE OF PROACTIVE REPLACEMENT OF QUESTIONABLE PARTS.
- CREATE "INTELLIGENT" POWER SYSTEMS THAT CHANGE THEIR CONFIGURATION BASED UPON REAL-TIME SYSTEM OPERATING NEEDS, LEADING TO HIGHER EFFICIENCY – SLEEP MODES, FOR EXAMPLE.

These types of solutions will most likely only be applied in "high end" systems at the present time. However, as more experience is gained, it is expected that they will migrate down into more cost sensitive application in future years. In any event, the possibilities are quite exciting.

6. MOVING FORWARD WITH ERICSSON

Ericsson has over 23 years of experience with board mounted power conversion at both the power module and system levels. Many of the control ICs used in Ericsson converters have been designed internally. We are perhaps the only remaining large supplier of power conversion products to the OEM market that maintains its own system level expertise through active participation in the design of telecom systems. This experience base has allowed us to successfully collaborate with our many customers over the years and has resulted in power system designs featuring world class levels of efficiency and reliability. We will continue this emphasis on collaboration as we enter the era of digital control and management. As a beginning, we are expending considerable effort in the development of standards and industry awareness through the following forums:

- MEMBERSHIP IN SM-IF, THE OWNER OF THE PMBUS SPECIFICATION
- MEMBERSHIP IN BOTH DOSA AND POLA FOR THE PURPOSE OF DEFINING STANDARDIZED PRODUCTS AND INTERFACES
- ACTIVE PARTICIPATION IN IEEE FORUMS AND CONFERENCES
- CUSTOMER EDUCATION VIA DESIGN AND APPLICATION NOTES

While the digital power revolution is young and many details will necessarily develop over time, there are some guiding principles that Ericsson will be emphasizing:

- EFFICIENCY IS KEY FOR OUR CUSTOMERS. WE WILL CONTINUE TO EMPHASIZE IT IN OUR NEW DESIGNS, WITH AN EMPHASIS ON "DESIGN FOR THE ENVIRONMENT" – THAT IS, MINIMIZING THE TOTAL POWER CONSUMPTION DURING OPERATION OF THE APPLICATION.
- DIGITAL CONTROL AND/OR MANAGEMENT WILL BE ACCEPTED ONLY IF IT PROVIDES VALUE TO THE END USER. FOR A COMPARABLE COST LEVEL, IT MUST PROVIDE MORE FUNCTIONALITY OR PERFORMANCE THAN THE CORRESPONDING ANALOG SOLUTION.
- CUSTOMERS MUST NOT BE FORCED TO ADOPT DIGITAL POWER MANAGEMENT AT THE SYSTEM LEVEL. POWER CONVERTERS WITH INTERNAL DIGITAL CONTROL SHOULD BE ABLE TO BE USED IN SYSTEMS JUST LIKE ANY CONVENTIONAL CONVERTER WITH ANALOG CONTROLS.

- IF CUSTOMERS CHOOSE TO IMPLEMENT DIGITAL POWER MANAGEMENT AT THE SYSTEM LEVEL, IT SHOULD BE EXTREMELY FLEXIBLE. THE CUSTOMER SHOULD HAVE A CHOICE OF USING IT ONLY DURING PRODUCT DEVELOPMENT, DURING SYSTEM ASSEMBLY AND TEST OR IN THE FIELD.
 - CUSTOMERS WHO USE THE PMBUS FOR SYSTEM POWER MANAGEMENT SHOULD BE SUPPORTED BY THE BEST POSSIBLE DESIGN TOOLS.
 - WORK WITH OTHER PMBUS MEMBERS FOR THE DESIGN OF A STANDARDIZED GUI FOR DEVELOPMENT AND TESTING PURPOSES.
 - PROVIDE EVALUATION BOARDS THAT DEMONSTRATE THE POWER AND CONVENIENCE OF THE PMBUS INTERFACE.
 - DEVELOP STANDARDIZED PROCESSES FOR MANAGING THE SOFTWARE AND FIRMWARE REQUIREMENTS OF DIGITAL POWER. ERICSSON ALREADY HAS EXTENSIVE EXPERIENCE WITH THIS FROM TELECOM EQUIPMENT.
 - CONTINUED ACTIVE PARTICIPATION IN POLA AND DOSA, BOTH FOR PURPOSES OF PRODUCT DEFINITION AND CUSTOMER EDUCATION AND SUPPORT.
 - CONTINUE TO ACTIVELY CHAMPION STANDARDS WHILE STILL ALLOWING FOR DIFFERENTIATION IN PRODUCT OFFERINGS AND TECHNOLOGICAL DEVELOPMENT.
- Ericsson's commitment for customer collaboration and support will be a focus as we begin to roll out digitally controlled products. We see many possibilities in this regard, including:
- INSURE DATA INTEGRITY IN THE PMBUS ENVIRONMENT BY MEANS OF RIGOROUS QUALIFICATION TESTING BASED ON EXPERIENCE FROM OTHER DIGITAL COMPONENTS IN ERICSSON'S TELECOM EQUIPMENT.
 - ERICSSON'S EXISTING EXPERIENCE WITH FIRMWARE PROGRAMMING WILL BE LEVERAGED BY PARTNERSHIPS WITH TIER ONE SEMICONDUCTOR MANUFACTURERS AND SUPPLIERS OF DIGITAL PWM CONTROLLERS.
- We invite our customers to join us as a collaborative partner for progress. We want our customers to feel secure with both our products and our support as they move forward with Ericsson.

Combining our strengths A True Collaborative Partner for Progress

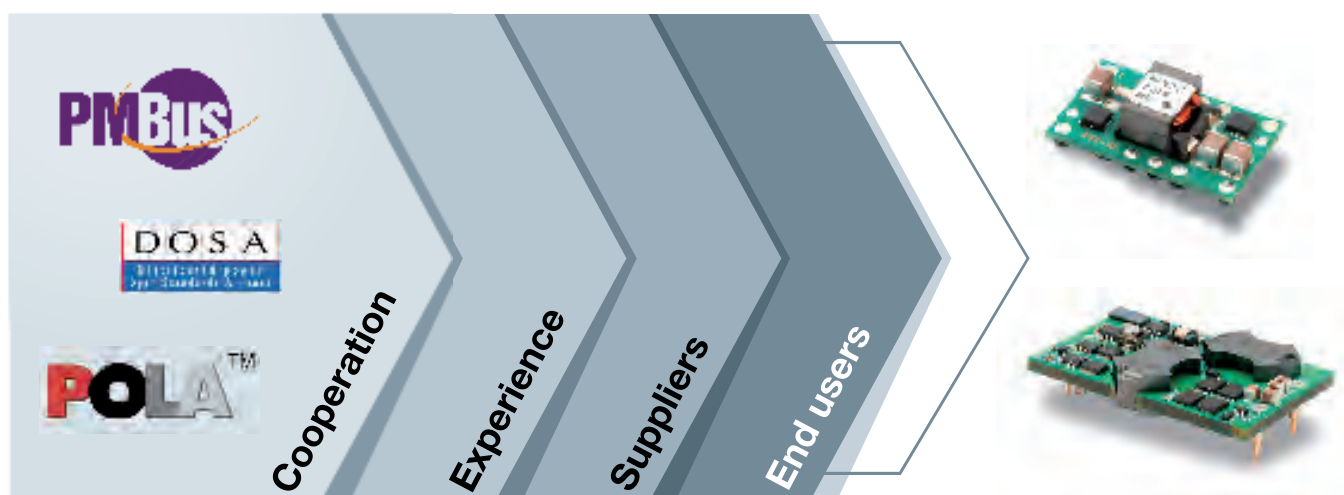


Figure 18 – Ericsson will use a collaborative approach together with partners, suppliers and customers to realize the benefits of digital power.

7. GLOSSARY

Analog	A variable signal that is continuous in both time and amplitude	OCP	Over Current Protection
ADC	Analog to Digital Converter	OEM	Original Equipment Manufacturer
ATE	Automated Test Equipment	OTP	Over Temperature Protection
CMOS	Complimentary Metal Oxide Semiconductor	OVP	Over Voltage Protection
DC	Direct Current	PMBus	Power Management Bus
Digital	A signal or system that uses discrete levels or numbers, often binary, for information representation	POL	Point of Load
DOSA	Distributed-power Open Standards Alliance	POLA	Point of Load Alliance
EEPROM	Electrically Erasable Programmable Read Only Memory	Power Control	Control of the energy transfer inside a power converter
FPGA	Field Programmable Gate Array	Power Management	Control and/or monitoring of the behavior of one or more power converters within a power system
GUI	Graphical User Interface	PWM	Pulse Width Modulator or Pulse Width Modulation
IC	Integrated Circuit	RAM	Random Access Memory
I2C	Inter-IC Bus	ROM	Read Only Memory
IP	Internet Protocol	SMBus	System Management Bus
MOSFET	Metal Oxide Semiconductor Field Effect Transistor	SM-IF	System Management Interface Forum
MUX	Multiplexer	TCP/IP	Transmission Control Protocol / Internet Protocol
		μC	Micro Controller

8. REFERENCES

- [1] “Real Performance Improvements for OEM System Designers: A Digital Control Case Study”, Digital Power Forum 2006, Torbjörn Holmberg, Per-Johan Wiberg, Ericsson Power Modules
- [2] “The Next Steps for Digital Control”, Digital Power Forum 2005, Bob Carroll, Primarion
- [3] Power Management Bus (PMBus) Implementers Forum <http://www.pmbus.org>
- [4] System Management Interface Forum (SMIF) <http://www.powersig.org>

All referenced papers and data sheets can be found at Ericsson Power Modules' web site: <http://www.ericsson.com/powermodules>

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ERICSSON

REDUNDANT MICROTCA POWER SYSTEMS

The demanding requirements put forth by redundant operation for both payload and management power can be met and interoperability between the power modules and the MicroTCA carrier hub achieved using MicroTCA compliant products.

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ABOUT THIS PAPER

The material contained in this paper was first presented on June 3rd, 2008 at the MicroTCA conference.

This focused one-day international conference served an audience of decision makers who are interested in learning about and contributing to the latest practical advancements related to the use of MicroTCA systems and components. The conference targeted hardware & software designers, engineering managers, system integrators and product managers.

1. INTRODUCTION

The Micro Telecommunications Computing Architecture (MicroTCA™) platform is becoming increasingly popular as a packaging solution for small to intermediate sized Information and Communications Technology (ICT) equipment. It offers several benefits for these types of systems, including high performance, design flexibility, high availability configurations and cost effectiveness. The MicroTCA specification defines requirements for the power system components, including the MicroTCA power module (PM), which contains the majority of the power generation and control functionality for the system. The specification contains stringent requirements for the power module when redundant power modules are utilized to achieve high availability system operation. This paper will present the results of a case study on using standard Ericsson PMs in a redundant configuration.

An overview of the MicroTCA power architecture will be provided along with a summary of the PM design requirements as they relate to redundant operation. This will be followed by a description of how these requirements are implemented with Ericsson's PM design. Finally, results of performance verification testing will be provided that demonstrate how the Ericsson design meets the demanding requirements of redundant operation for both payload and management power, including loss of input power, PM failure and hotswapping. The testing will also demonstrate that interoperability is achieved between the PMs and the MicroTCA Carrier Hubs (MCH) during the interval of handing over system power responsibility from one PM to another.

This paper is intended for a wide audience including MicroTCA OEM system integrators, engineers involved with selecting, evaluating and testing of PMs, and manufacturers of MCHs. The results provided should enhance the confidence level that these designs can indeed meet the stringent requirements of 1+1 redundancy, including transitioning through a power failure without interruption of system payload and management power. Increased credibility in the overall MicroTCA platform concept should also be achieved, in terms of demonstrating interoperability between different components and suppliers. It will be shown that standard MicroTCA components that are in compliance with the specification can achieve all of the difficult objectives associated with redundancy without the need to resort to expensive and risky customized solutions.

2. MICROTCA POWER REQUIREMENTS OVERVIEW

This section is intended to provide a brief summary of the requirements for a MicroTCA power system, with a focus on the PM specifications as they relate to redundant operation. The information included is from the MTCA.0 R1.0 version of the MicroTCA specification [1]. Additional information about the power implementation of the MicroTCA platform can be found in reference [3]. This paper only addresses redundancy as it applies to payload and management power. Some high availability MicroTCA systems may also extend redundancy into the AC/DC front-ends and input power distribution, but these techniques are outside the scope of this discussion.

The MicroTCA platform requires all payload circuitry to reside in AdvancedMC™ (AMC) modules and centralizes all the main power conversion/control functions for a sub-rack into one or more PMs. The overall architecture of a MicroTCA system is shown in Figure 1. The system as shown in the figure supports up to a maximum of 12 AMC modules which contain the payload circuitry, and each of these AMCs is specified to require from 20 to 80 watts of payload power. The MCH function provides overall control for the interconnected AMCs. A second redundant MCH is often added for systems with high availability requirements. Similarly, a second redundant cooling unit (CU) is sometimes used. The backplane is used as an interconnection mechanism for all of these elements.

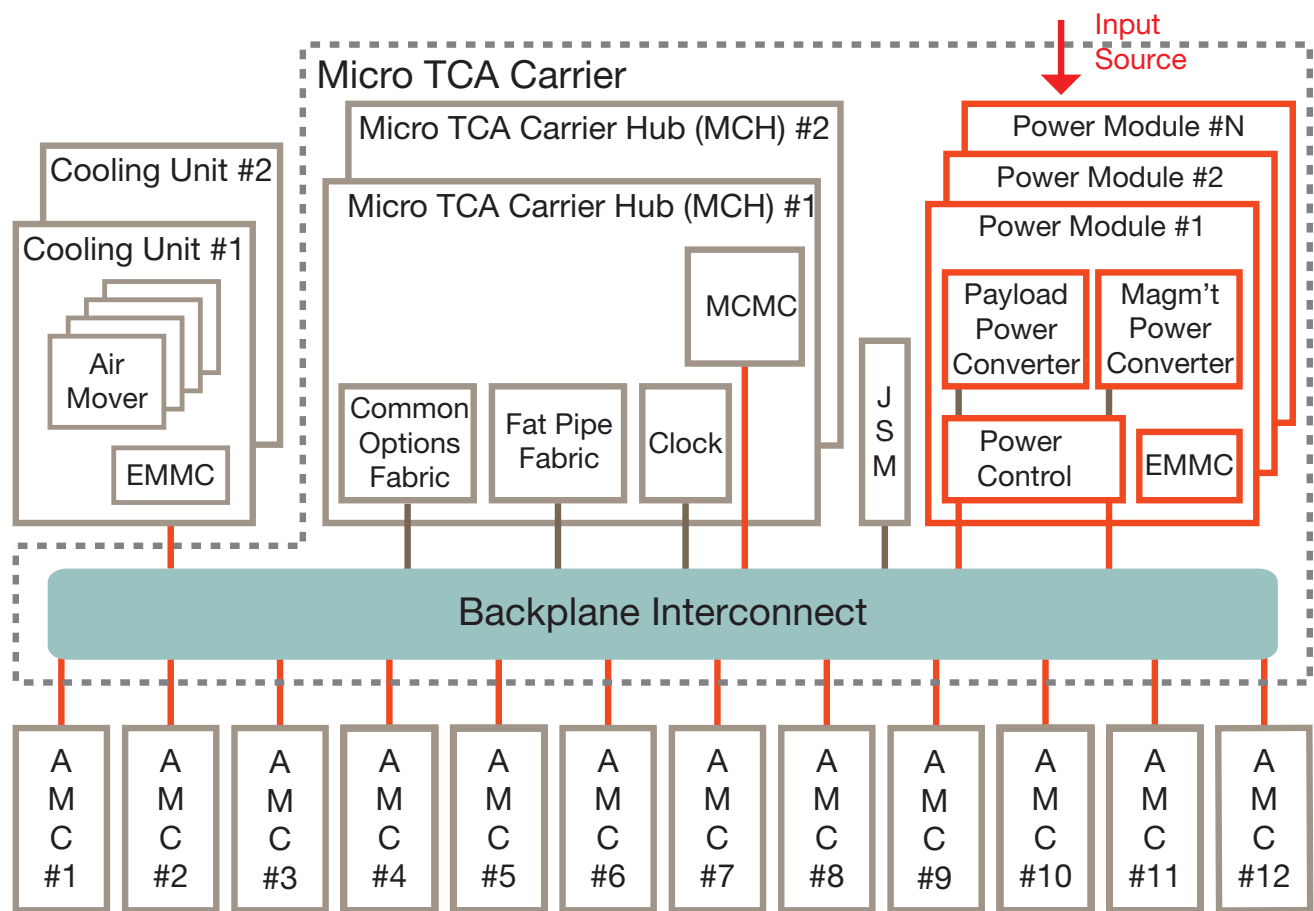


Figure 1 - MicroTCA block diagram with parts of the power system highlighted

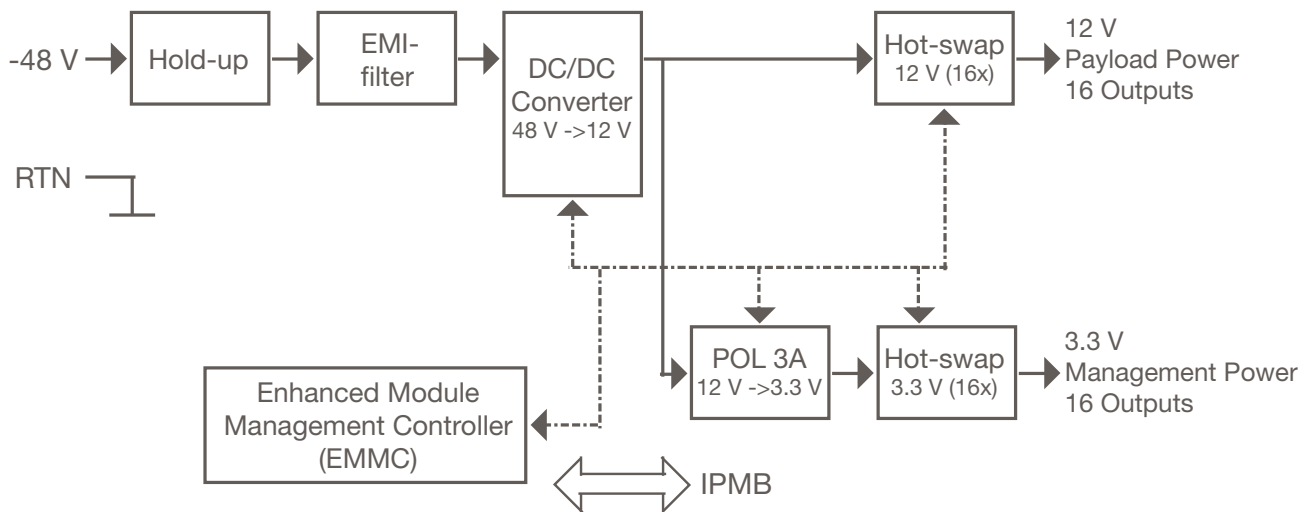


Figure 2 - Example of MicroTCA power module block diagram

The power module is a very key element in the overall MicroTCA system. It serves as a centralized power conditioning, conversion and control block for the entire sub-rack. Anywhere from one to four power modules may be used in a single MicroTCA system with more than one being used either because of the power demand or because of a desire for redundancy. The PM provides payload power at a nominal 12 V level and management power at a nominal 3.3 V. In addition to supplying payload and management power to up to 12 AMCs, the PMs must be capable of supplying payload and management power to up to two CUs and two MCHs. As a consequence, many PMs are designed to provide a total of 16 output power channels, or 32 channels if payload and management power are considered separately. A block diagram of a typical PM is shown in Figure 2. A photograph of the Ericsson PM used in this case study is provided in Figure 3 together with a summary of its specifications. Additional detail regarding the overall design and functionality of the PM can be found in reference [2].

The MicroTCA specification includes provision for redundant PMs to increase system availability in critical applications. The specification contains very specific requirements for the implementation of power module redundancy. Techniques such as power paralleling and current sharing are not used, and only one power module may deliver current to any load channel at any given time. This architectural restriction was established so that the maximum overcurrent possible to any channel is limited. If two power modules were paralleled, the maximum fault current could be doubled, which would expose the system backplane and connectors to excessive current and possibility of damage.

MicroTCA PMs are defined as either “primary” or “redundant”. One or more primary PMs supply the payload and management power under normal system operating conditions. Each system can contain one redundant PM that takes over for a failed primary PM.



OUTPUT POWER	355 W
INPUT POWER	385 W
OUTPUT VOLTAGE CHANNELS	16 X 12 V AND 16 X 3.3 V
EFFICIENCY AT 50% LOAD	95%
NORMAL INPUT VOLTAGE (FULL PERFORMANCE)	-40.5 V TO -57 V
HOLD-UP (-54 V IN)	8 MS
CONDUCTED EMISSIONS	CLASS B
FORM FACTOR	FULL SIZE (6HP) SINGLE-WIDTH

Figure 3 - The Ericsson MicroTCA power module ROA 117 5078/1

After this transition is complete, the former redundant PM then acts as the primary PM for the assigned loads. It is important to understand that any given PM is either primary or redundant at any given time. It cannot simultaneously provide both roles. The specification requirements can be summarized as follows:

- ONE PM IS ASSIGNED TO BE REDUNDANT. ALL OTHER PMS ARE PRIMARY.
- THE MCH CANNOT ASSIGN ANY CHANNELS ON THE REDUNDANT PM TO BE THE PRIMARY POWER SOURCE FOR ANY LOAD.
- THE MCH ASSIGNS A CHANNEL FROM ONE OF THE PRIMARY PMS TO BE THE PRIMARY SOURCE OF PAYLOAD AND MANAGEMENT POWER FOR A LOAD.
- THE MCH ASSIGNS THE CORRESPONDING CHANNEL ON THE REDUNDANT PM TO BE THE REDUNDANT SOURCE OF PAYLOAD AND MANAGEMENT POWER FOR THAT SAME LOAD.
- IN THE EVENT OF A FAILURE ON A PRIMARY PM, THE REDUNDANT PM AUTOMATICALLY TAKES OVER THE LOADS FROM THE PRIMARY PM AND SIMULTANEOUSLY DISABLES ALL OTHER CHANNELS.
- THE REDUNDANT PM THEN BECOMES A PRIMARY PM.

This methodology becomes more understandable when looking at some examples. *Figure 4* depicts a system that is configured with 2+1 redundancy.

In this system, two PMs are used to supply both payload and management power to a total of 16 output channels. A third PM is normally in a stand-by state and is available to provide power to any of the 16 channels (32 voltage outputs) in the event of a fault in either of the two main power modules. PM 1 supplies the normal power to only channels 1 through 8, while PM 2 does the same for channels 9 through 16. The redundant PM 3 can supply power to any of the 16 output channels, but only in case of failure in one of the primary PMs or if one of the two has been disabled.

A 1+1 redundant system is shown in *Figure 5*. In this case the primary PM powers the entire system and the redundant PM is in stand-by mode so that it can take over in the event that there is a failure on one or more channels of the primary PM. After this

transition, it then is assigned as the primary PM. This 1+1 system is the basis for the performance verification testing that will be described later in this paper.

Automatic transition between a failed primary power module and the redundant power module is accomplished by the settings of their output voltages. Primary PMs are set to a higher output voltage than redundant PMs, the two payload ranges being 12.25 to 12.95 V for primary PMs and 11.60 to 12.00 V for redundant PMs. An O-Ring function internal to the PM, to be described in the next section, along with the voltage budgets insures that the PM with the higher output voltage (normally the primary PM) supplies the entire load power and that the other PM (normally the redundant PM) is unloaded. In addition, it is required that all PMs contain sufficient energy storage such that there is a voltage droop of less than 1 V during the transition process from the primary to the redundant PM. These specifications are for the payload power, but a similar set of requirements are defined for management power. This paper addresses the payload power since the higher current levels associated with it makes it the more demanding specification to meet. But the implementation presented here also successfully meets all the requirements for management power delivery.

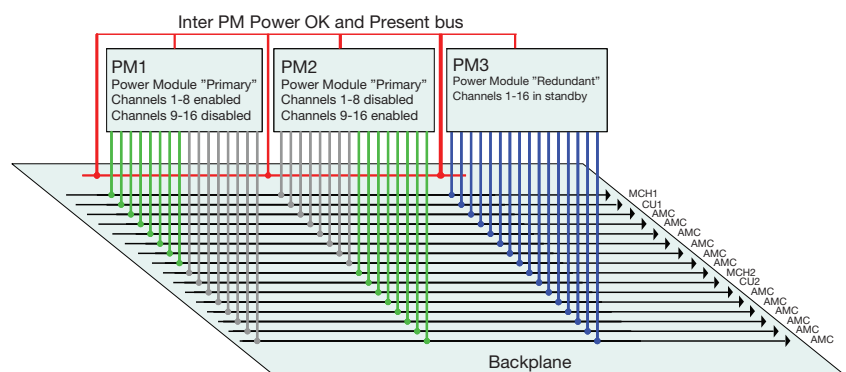


Figure 4 - Example of 2+1 redundant MicroTCA power module implementation

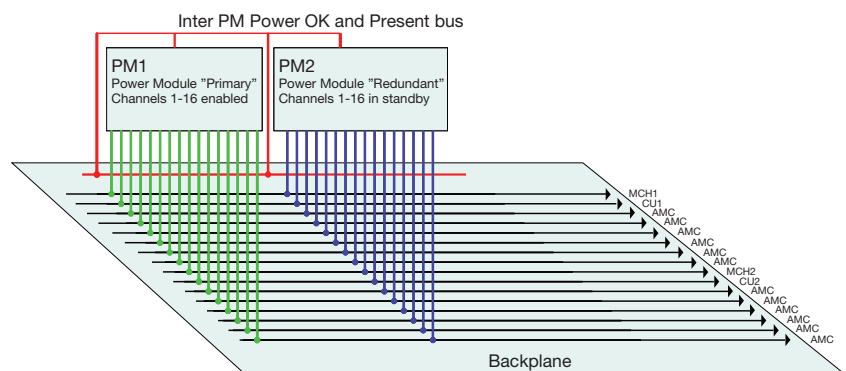


Figure 5 - Example of 1+1 redundant MicroTCA power module implementation

The droop requirement is in place to insure that the operation of the payload and management loads are not affected by the transition to a redundant PM. The 1 V specification can be confusing, given the voltage budgets provided. Ericsson interprets the specification to mean that there should be less than a 1 V dip below the nominal DC setting of the redundant PM. Furthermore, the Ericsson design insures that the minimum transitory voltage is never lower than 10.8V at the input to an AMC. This still provides a significant margin above the specified minimum AMC input voltage which is 10.0V.

The MicroTCA redundancy specification requirements described above were developed due to several system-level considerations. One was the desire to limit the maximum current in the backplane and connectors. If two PMs could be active for any given output channel, the fault current could be twice that of a single PM. Secondly, the backplane is not a replaceable component in the field. Consequently, it is important to keep it completely passive with no active components on it so that its reliability is maximized. This restriction prevents O-Ring diodes to be mounted on the backplane and prevents the use of conventional current sharing techniques. Thirdly, the transition to a redundant PM must be instantaneous in the event of a primary PM failure. This precludes the MCH from signaling the redundant PM to start up, since the delay in the output voltage ramp-up would be excessive. Therefore, the redundant PM must be turned on at all times so that it can provide power immediately when needed.

3. ERICSSON POWER MODULE IMPLEMENTATION

The preceding section summarized the design requirements for the PM as defined by the MicroTCA specification. This section will examine some details of the actual implementation of those requirements within the Ericsson PM shown in *Figure 3*. Ericsson includes some cutting edge technology in this product that will differentiate it in terms of performance, reliability, packaging density and user flexibility/configurability. This discussion will address primarily the payload channel power control implementation and the capabilities and performance of the DC/DC converter selected to provide the main payload power conversion function.

3.1 CHANNEL POWER CONTROL

Figure 6 is a simplified diagram showing the implementation of the payload channel power control function. The Enhanced Module Management Controller (EMMC) is a digital device that interfaces the power control functionality within the PM to the remainder of the MicroTCA system. This diagram shows only one of the 16 payload channels. There are also 16 similar management power channels that are not shown. In each PM, therefore, the current sensing resistor, O-Ring and pass transistors and the power control block functions are replicated 32 times. The power control block shown between the EMMC and the current sense resistor and output control transistors consists primarily of a hotswap control integrated circuit (IC). These ICs can handle multiple channels, so the number of chips required will vary but the described functionality is independently required for each of the 32 output voltage channels.

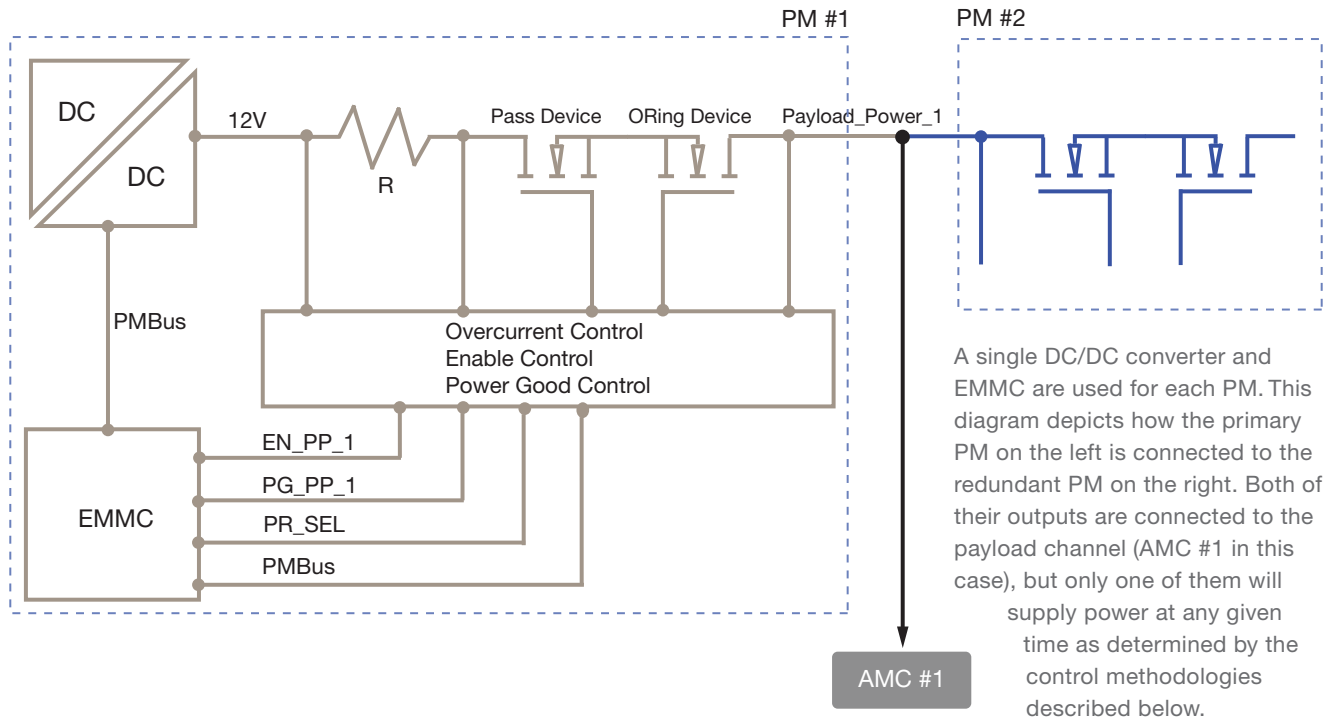


Figure 6 - Example of payload channel control that allows for redundant operation

Each channel has two semiconductor switches in series. The O-Ring device prevents current from flowing in the reverse direction from the load into the power module. The pass device is used to enable or inhibit the output current and also to limit the value of the current to provide for functions such as soft start for hotswap and fault current limiting. The primary PM has both the pass and the O-Ring devices turned on to provide the lowest resistance current flow to the load. The redundant PM will have the pass device turned on so that it is ready to instantaneously deliver current if needed. Its O-Ring device, however, will be turned off to prevent any current flow into the redundant PM from the higher voltage level primary PM. In the event of a failure of the primary PM, the O-Ring device of the redundant PM can instantaneously provide current to the load through its intrinsic body diode. This connection will then be made more efficient by turning on the O-Ring device of the redundant PM to decrease its channel resistance when it becomes the primary PM.

Figure 6 also depicts two connections implemented with a Power Management Bus (PMBus™). The PMBus is a bidirectional serial digital bus that is central to the implementation of systems using digital power control and digital power management. This paper only describes its usage for this application, but additional information about the PMBus can be found in reference [6]. In this implementation the PMBus between the EMMC and the power control block is used so that the EMMC can monitor and change settings of the power control block during operation. The PMBus connection between the EMMC and the DC/DC converter is used so that the DC/DC converter can be programmed for the proper output voltage corresponding to its function as either a primary or redundant PM. The EMMC may also collect data on output current and temperature from the DC/DC converter. There is also, as depicted in Figures 4 and 5, an interconnection between the PMs so that each knows if the other is present in the system and its power good status.

FORM-FACTOR	¼-BRICK (2.28" X 1.45")
INPUT VOLTAGE	36 - 75 V
OUTPUT VOLTAGE	12 V ±2%
OUTPUT POWER	400 W
EFFICIENCY	96.5% AT 50% LOAD
CONTROL IC	DIGITAL µC
COMMUNICATIONS INTERFACE <ul style="list-style-type: none"> - MONITOR TEMPERATURE, CURRENT AND VOLTAGE - CONFIGURE WARNING/FAULT SET POINTS - CONTROL V_{OUT} SET POINT, ENABLE/DISABLE 	

Figure 7 - The digitally controlled Ericsson BMR453 DC/DC converter

3.2 DC/DC CONVERTER

As described previously, tightly controlled output voltage tolerances from the DC/DC converter are required in order for the PM redundancy feature of the MicroTCA platform to function properly. The Ericsson PM design uses the BMR453 DC/DC converter [8] that incorporates several breakthroughs in terms of performance and functionality. It is capable of digital power management via its PMBus interface, allowing on-the-fly adjustment of output voltage so that it can be defined as either a primary or redundant PM without interruption of power to the system. This same interface can also be used to collect useful data from the DC/DC for the purpose of communicating it to the rest of the system and to the outside world. This capability is useful for measuring values of such parameters as output current and operating temperature. The PMBus can also be used in the other direction for the purpose of modifying the DC/DC parameters and behavior during engineering development and system test. Fault limit set points and expected responses for such items as over current, over voltage and over temperature are a frequently used example of this capability.

The output voltage budget for implementing redundancy requires an output voltage accuracy from the DC/DC converter of +/- 2%. This requirement demands that a fully regulated converter be used so that both line and load variations as well as temperature effects can be compensated for, and prevents the usage of less complex converter topologies such as those used in more loosely regulated Intermediate Bus Converters (IBC). Fully regulated DC/DC converters traditionally exhibit significantly less power density and efficiency than IBCs. The Ericsson DC/DC converter design in these PMs smashes these barriers. Due largely to the digital control methodologies used in its design, the parts count is drastically reduced and it delivers power density and efficiency equivalent to the best IBCs while still being cost-effective to manufacture. It can deliver up to 400 watts of output power (payload and management channels combined) from a ¼ brick sized package. The operating efficiency is 96.5% at half load and 95.5% at full load, making it one of the most efficient converters available. Its output regulation including line, load and temperature effects is within +/- 2%. Photographs of this DC/DC converter along with a summary of its performance parameters are shown in Figure 7. More information about the DC/DC converter design is available in references [4] and [5].



4. PERFORMANCE VERIFICATION

Previous parts of this paper have defined the requirements for redundancy as set forth in the MicroTCA specification and summarized Ericsson's strategy and designs for meeting these requirements. Now it is time to see if it works in the "real world". The purpose of this case study is to place the Ericsson standard PM into a standard MicroTCA enclosure along with AMC loads and a MCH and then verify that it meets the redundancy requirements for high availability when exposed to fault and maintenance conditions. The enclosure, MCH and AMC cards are all standard units from suppliers other than Ericsson. Test results will be shown for two scenarios – loss of input voltage or PM failure, and a hotswap maintenance action.

A block diagram of the MicroTCA system used for these tests is shown in Figure 8. The highlighted areas represent the hardware installed in the enclosure, which is a 14 slot MicroTCA sub-rack. Two Ericsson ROA 117 5078/1 PMs are installed in the rack along with 8 Elma AMC load boards and a standard NAT MCH. The nominal input voltage to the PMs is -54 V at a power level of 383 W. The AMC load boards consist of resistive loads. As a consequence, their power dissipation will be dependent on their input voltage, and they will dissipate less power when operated from the lower voltage of a PM in redundant mode. That is why they are listed as 40 to 45 W each. Each load board also has 20 μF of input capacitance to simulate the minimum specified AMC decoupling capacitance for a 40 W AMC [7]. A photograph of such a setup is shown in Figure 9. Although not completely identical to the test system used here, it provides perspective as to the size and configuration of the system. The 8 AMCs are clearly visible as are the Ericsson PMs at both ends of the enclosure.

4.1 LOSS OF INPUT VOLTAGE OR POWER MODULE FAILURE

The primary reason for using a redundant configuration of PMs in a MicroTCA system is so that the system can operate through an unexpected failure of one PM. This type of failure could have several root causes, but the two most likely are either a random failure internal to the PM or loss of input DC power to the PM because of an intermittent connection or other problem with the front-end power generation or distribution. Both of these failure modes can be simulated in the test system by pulling out the -48V input power cable from the primary PM while the system is operating. This will disable the DC/DC converter in that PM and create the same error indications that would occur if there were a random failure in the PM. Ideally, the redundant PM will automatically take over for the primary PM without any disruption of power to the AMC loads.

The results of this test are shown in Figures 10 and 11.

Focusing first on Figure 10, it shows three waveforms. The upper one is the voltage on one of the AMC channels. Initially the voltage is at about 12.5 V, which is the nominal set point of the primary PM less the DC distribution drops. Note that the voltage levels shown in this section represent the AMC input voltage, which is slightly lower than the PM output due to the backplane distribution losses. The center waveform is the DC input current to the primary PM. Its initial value is 7.1 A, since at this point the all of the output power and current to the system.

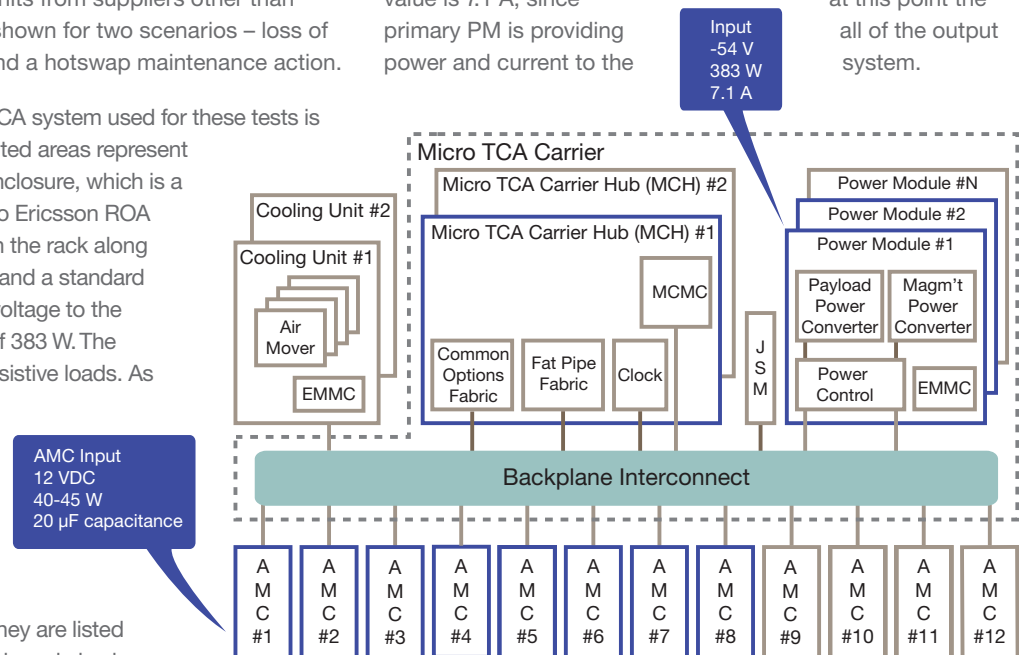


Figure 8 - Block diagram and devices used in the test setup



Figure 9 - Photo of MicroTCA system with test equipment for measuring current and voltage levels

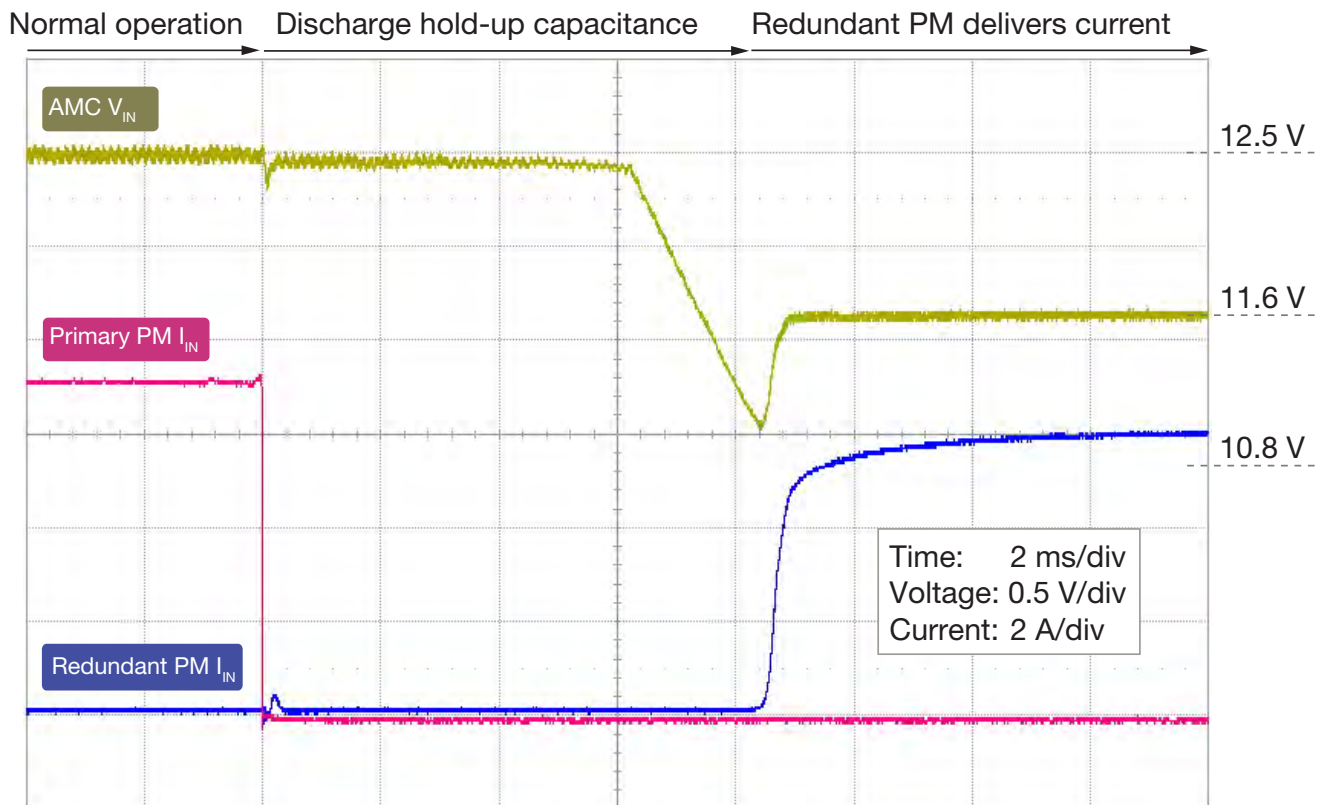


Figure 10 - Redundancy test #1 with 2 ms/div time scale, disconnecting -48 VDC cable

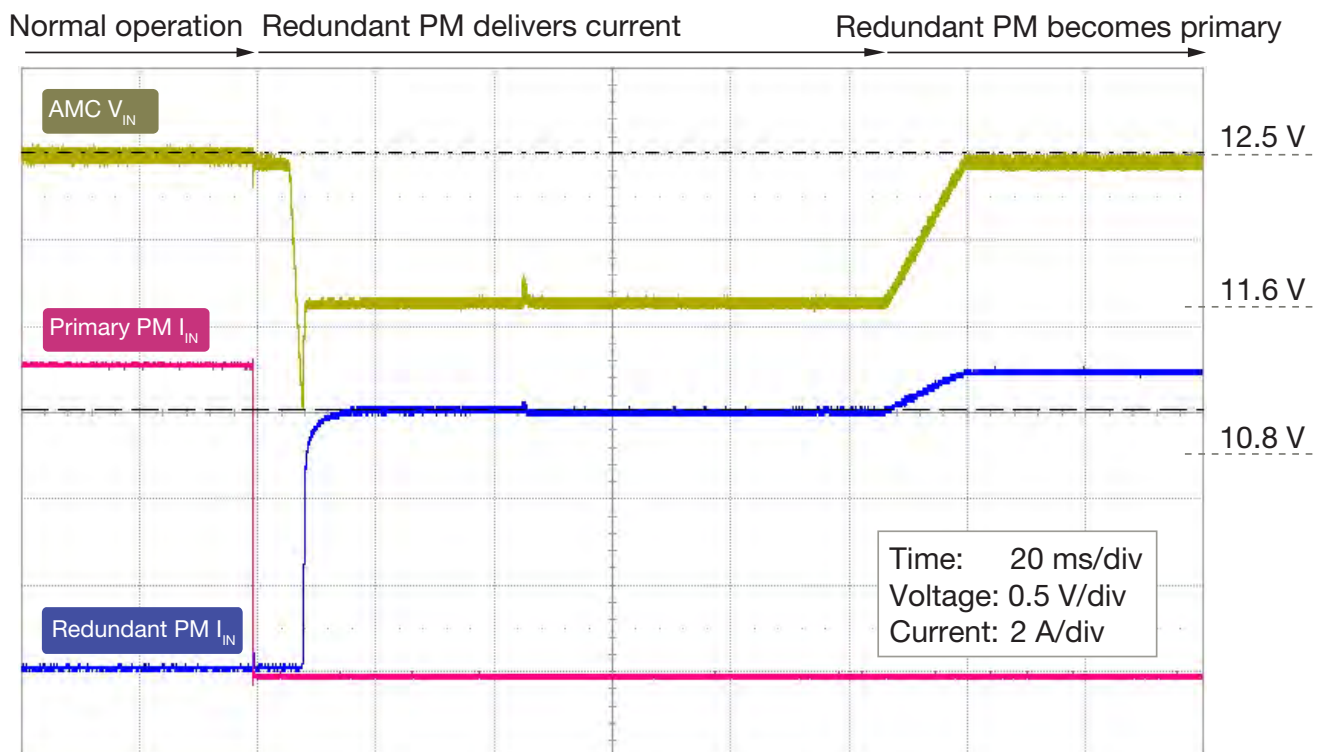


Figure 11 - Redundancy test #1 with 20 ms/div time scale, disconnecting -48 VDC cable

The lower trace is a similar measurement of the DC input current to the redundant PM. It appears to be zero, but the reader should keep in mind that at this point the redundant PM is turned on and operational, but is operating at zero output load because its O-Ring device is turned off. Because of the efficient “overhead” circuitry in the redundant PM, its input current appears in this view to be zero although it is actually a few milliamps.

The point at which the DC input power cable of the primary PM is removed is clearly visible in the figure as the primary PM input current goes instantly to zero. For the next few milliseconds the AMC input voltage will be supported by means of hold-up capacitance. For the first 6 ms, the AMC input voltage remains constant at about 12.5 V. During this time the primary PM DC/DC converter remains operating, taking its input current from the hold-up capacitance in the front-end of the PM. Since the PM DC/DC converter is fully regulated and operates down to an input voltage of 36 V, there is sufficient energy in the system to provide steady voltage to the AMC at full output current as the input hold-up capacitance discharges from the nominal 54 V to 36 V. When the primary PM DC/DC converter input voltage reaches 36 V, it shuts off. This event is evident in the upper trace as the AMC input voltage begins a downward decay. This decreasing input voltage is due to energy being drawn from the capacitance on the output of the primary PM and on the AMCs, and lasts for a little over 2 ms. Note that during this entire 8 ms period the input current to the PMs is

either zero (in the case of the primary PM) or insignificant (for the redundant PM), and the entire system is being powered from energy stored in capacitance.

When the AMC input voltage reaches the set point of the redundant PM, the body diode in its O-Ring device becomes forward biased and it begins to deliver current to the AMCs. This is a very stringent test for the PM, as its output load goes from zero to full load essentially instantaneously. This takeover of power delivery by the redundant PM is indicated in *Figure 10* by two events. There is a sudden rise in the redundant PM input current and there is an increase in the AMC input voltage to 11.6 V, which is the set point of the PM in its redundant role. Note that at no time does the AMC input voltage reach 10.8 V, the value Ericsson has selected to insure adequate margin for the minimum allowable 10.0 V value of the AMC input specification. At the end of the time interval depicted in *Figure 10*, the PMs have not switched roles. Even though the redundant PM is delivering all of the system power, it is still defined and operating as a redundant PM and is supplying output power at a lower voltage than a primary PM.

The transition of its role from a redundant to a primary PM can be observed by simply changing the time scale of the scope traces, as shown in *Figure 11*. In this figure, the time base is set at 20 ms/div. It can be seen that the system continues to operate as it was during the end of *Figure 10* for about another 100 ms. When the redundant PM begins to deliver current, it notifies the MCH.

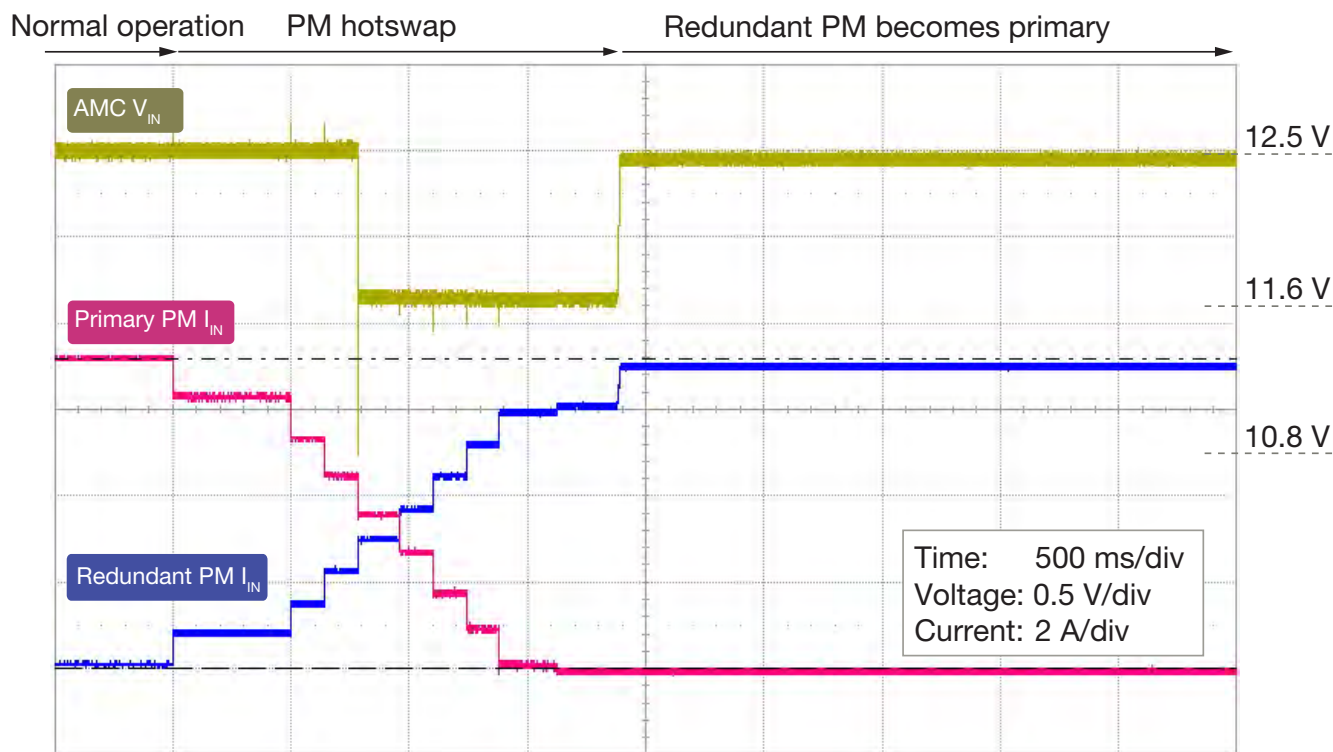


Figure 12 - Redundancy test #2 with 500 ms/div time scale, PM hotswap handling

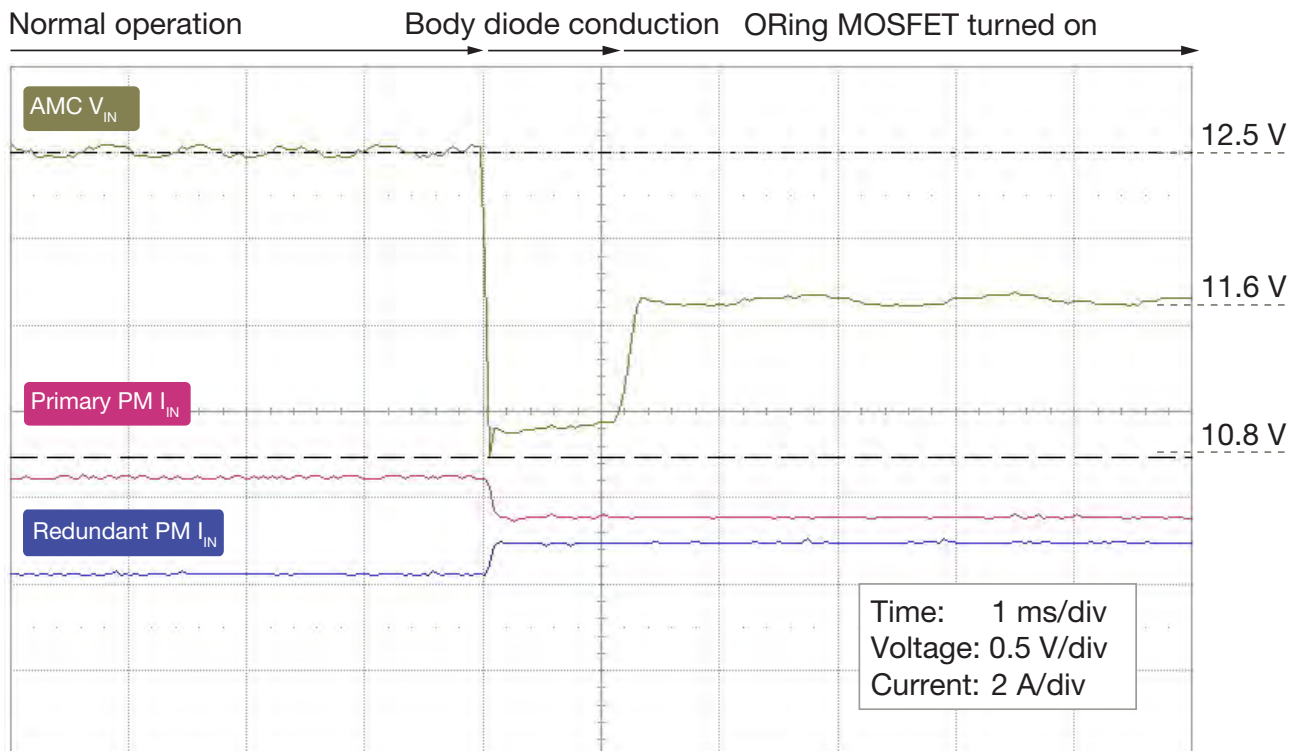


Figure 13 - Redundancy test #2 with 1 ms/div time scale, PM hotswap handling

Because of the interconnection between the PMs shown in *Figure 4 and 5*, the redundant PM will be aware that the PM_OK signal of the primary PM has gone down, indicating a failure. At this point, the redundant PM assumes the role of primary PM and increases its output voltage accordingly. This transition can be seen clearly in *Figure 11* as an increase in the AMC input voltage to 12.5V. There is also a slight increase in the now primary PM's input current due to the increase in output power from increasing the voltage on the resistive load. All of this can be accomplished in much less than 100 ms, but there is a built-in 100 ms "debouncer" before the role transition so that transient noise and glitches can be filtered out.

This test successfully demonstrates that unexpected PM or input voltage failures can be automatically accommodated by the redundant PM configuration without affecting the operation of the AMC loads.

4.2 HOTSWAP

Redundant MicroTCA systems are configured so that a PM may be replaced in the field without disrupting operation of the system. This type of maintenance action would be initiated if it was felt that a given PM was degrading in performance or if PMs were replaced for upgrade purposes. In this case we are dealing with a deliberate action rather than the unplanned result of a failure as in the preceding test. The same scenario is applicable in systems where the MCH changes responsibilities between PMs to

balance the load over time and thus improve reliability. The test described here was done to verify that the AMCs operate without disruption during both maintenance replacement of a PM and also when the MCH decides to shift the role of the redundant PM.

In this test, the primary PM was hotswapped while the system was running. Each of the Ericsson PMs has a handle on its exterior faceplate that the user pulls to initiate extraction of the PM from the system. There is a sensor on the handle that tells the PM to initiate a hotswap sequence when the handle is activated, and the PM will then notify the MCH that it is about to be extracted from the system. Upon receiving this notification, the MCH will begin sending commands to the primary PM telling it to disable payload and management power. There will be one command issued per channel so that the deactivation can be done in a controlled manner to avoid large amounts of transient currents. As each channel is deactivated by the primary PM, the corresponding channel of the redundant PM automatically takes over supplying current to that channel. This operation can be seen in *Figure 12*. The scope traces in this figure represent the same connection points as in the previous two figures, the upper trace being the AMC input voltage and the lower two traces the input currents to the two PMs.

Note the staircase current waveforms as the power delivery for each of the eight channels is sequentially handed off

from the primary to the redundant PM, the entire process taking approximately 1.8 seconds. After the last channel of the primary PM has been deactivated, it is reset and a blue LED is activated on its front panel telling the user that it is safe to extract the PM. During the reset of the primary PM, the redundant PM sees that the PM_OK signal from the primary PM is gone, and then changes its role from redundant to primary and increases its output voltage. Note that the upper trace showing the AMC input voltage is arbitrarily connected to the fourth channel to be transferred from the primary to the redundant PM. Consequently, its voltage remains at 12.5 V until the fourth transfer and then is reduced to the redundant PM voltage level until the transfer of roles between redundant and primary, at which point it returns to 12.5 V. Other channels will see more or less time at the lower operating voltage.

It is instructive to take a closer look at the leading edge of the power transfer on this channel as shown in *Figure 13*. All the scope connections and vertical scaling remain the same as the previous figure and only the timebase is changed to 1 ms/div so that more detail of the actual power transfer may be seen. Note first of all that the channel voltage always remains above 10.8 V so that the MicroTCA AMC specifications are again given adequate margin. The voltage waveform also illustrates the behavior of the channel power control operation. When the channel is deactivated in the primary PM, there is a sudden drop in voltage as the redundant PM supplies current to the channel through its O-Ring device body diode. During this time, the redundant channel pass device is turned on and its O-Ring device is turned off. Within a millisecond, the O-Ring device is turned on to reduce the voltage drop and to increase the channel efficiency. It is clear from the scope trace that there is about 0.6 V less drop with the O-Ring device turned on. The redundant PM then continues to supply current at the reduced output voltage until it assumes the role of primary PM at the conclusion of the hotswap sequence and increases its nominal output voltage to 12.5 V.

This test successfully demonstrates that planned maintenance hotswap actions and MCH initiated transfer of primary / redundant roles during operation are supported by the MicroTCA redundancy specifications and the Ericsson PMs.

5. SUMMARY AND CONCLUSIONS

This case study demonstrates that standard MicroTCA components can be used to implement high availability systems by means of redundancy. A new high efficiency high power density DC/DC converter is described that is used within the standard Ericsson PM and is responsible for many of the industry-leading performance attributes of the PM. Specifically, it is shown that:

- ALL THE RELATED PROVISIONS OF MTCA.0 R1.0 CAN BE MET
- CONTINUOUS OPERATION IS MAINTAINED DURING
 - FAILURE OF A PM
 - LOSS OF INPUT POWER TO A PM
 - HOTSWAP OF A PM
 - MCH INITIATED TRANSFER OF ROLES
- INTEROPERABILITY IS ACHIEVED BETWEEN THE PM AND MCH
- THE DC/DC CONVERTER OFFERS A UNIQUE COMBINATION OF EFFICIENCY, POWER DENSITY AND OUTPUT VOLTAGE REGULATION
- CAPABILITY OF THE DC/DC TO ADJUST THE OUTPUT VOLTAGE DURING OPERATION AND MAINTAIN PRECISE REGULATION TOLERANCES IS KEY TO SUCCESS IN REDUNDANT APPLICATIONS

All of these objectives are met using only standard MicroTCA components. Components from various suppliers, if properly designed to the MicroTCA specifications, should successfully operate together to allow high availability solutions by means of PM redundancy. This is an important result, since the alternative would be to attempt customized proprietary power control implementations. In addition to being very labor intensive and expensive, proprietary solutions will increase technical risk and time-to-market. Approaches such as the one presented here represent a cost-effective method of achieving high performance, high reliability and availability and a streamlined system design process without the need for customized circuit design.

7. GLOSSARY

AMC	Advanced Mezzanine Card
CU	Cooling Unit
EMMC	Enhanced Module Management Controller
IBC	Intermediate Bus Converter
IC	Integrated Circuit
ICT	Information Communication Technology
LED	Light Emitting Diode
MCH	MicroTCA Carrier Hub
MicroTCA™	Micro Telecommunications Computing Architecture
OEM	Original Equipment Manufacturer
PM	MicroTCA Power Module
PMBus™	Power Management Bus

8. REFERENCES

- [1] MicroTCA base specification R1.0, PICMG, 6 July 2006
- [2] MicroTCA Power Module Preliminary Datasheet, Ericsson Power Modules, May 2008*
- [3] Advanced TCA Summit Europe 2007 - Performance, Cost and Reliability Considerations in a MicroTCA Power System*
- [4] APEC 2007 - Implications of Digital Control and Management for a High Performance Isolated DC/DC*
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- [6] Digital Power Technical Brief, Ericsson Power Modules, November 2006*
- [7] AdvancedMC base specification R2.0, PICMG, 15 November 2006
- [8] BMR453 DC/DC converter Technical Specification, Ericsson Power Modules, June 2008*

* All referenced papers and data sheets can be found at Ericsson Power Modules' web site: <http://www.ericsson.com/powermodules>

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ERICSSON

TECHNICAL SPECIFICATIONS

BMR 453 series Fully regulated Intermediate Bus Converters Input 36-75 V, Output up to 60 A / 396 W	EN/LZT 146 395 R6A July 2011
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Key Features

- Industry standard five pin Quarter-brick
57.9 x 36.8 x 11.6 mm (2.28 x 1.45 x 0.46 in.)
- Optional digital PMBus interface
- Fully regulated intermediate bus converter
- High efficiency, typ. 96% at half load, 12 Vout
- +/- 2% output voltage tolerance band
- 1500 Vdc input to output isolation
- 2.5 million hours MTBF
- Optional baseplate
- Optional output voltage Droop for parallel operation
- ISO 9001/14001 certified supplier
- PMBus Revision 1.1 compliant



Power Management

- Configurable soft start/stop
- Precision delay and ramp-up
- Voltage sequencing and margining
- Voltage/current/temperature monitoring
- Configurable output voltage
- Power good
- Synchronization
- Voltage track



Safety Approvals



Design for Environment



Meets requirements in high-temperature lead-free soldering processes.

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Ordering Information

Product program	Output
BMR4530002/003	3.3 V / 60 A, 198 W
BMR4530002/004	5 V / 60 A, 300 W
BMR4530000/002	9 V / 33 A, 297 W
BMR4530006/012	9.6 V / 33 A, 297 W
BMR4530000/001	12 V / 33 A, 396 W
BMR4530006/013	12 V / 33 A, 376 W
BMR4530006/014	12.45 V / 33 A, 391 W

Product Number and Packaging

BMR453	n ₁	n ₂	n ₃	n ₄	/	n ₅	n ₆	n ₇	n ₈
Mechanical pin option	x				/				
Mechanical option		x			/				
Hardware option			x	x	/				
Configuration file					/	x	x	x	x

Optional designation
Description

n ₁	0 = Standard pin length 5.33 mm 1 = Surface mount option ^{note 1} 2 = Lead length 3.69 mm (cut) 3 = Lead length 4.57 mm (cut) 4 = Lead length 2.79 mm (cut) 5 = Lead length 2.79 mm stand off 6.7 mm
n ₂	0 = Open frame 1 = Baseplate 2 = Baseplate with GND-pin
n ₃ n ₄	00 = 8.1-13.2 Vout With digital interface 01 = 8.1-13.2 Vout Without digital interface 02 = 3-6.7 Vout With digital interface 03 = 3-6.7 Vout Without digital interface 06 = 8.1-13.2 Vout With 0.6 V droop load sharing function Without digital interface 07 = 8.1-13.2 Vout With 0.6 V droop load sharing function With digital interface
n ₅ n ₆ n ₇	001 = 12 V Standard configuration 002 = 9 V Standard configuration 003 = 3.3 V Standard configuration 004 = 5 V Standard configuration 007 = 9 V with positive RC logic configuration 008 = 12 V with positive RC logic configuration 009 = 3.3 V with positive RC logic configuration 010 = 5 V with positive RC logic configuration 012 = 9.6 V with 0.6 V droop load sharing function configuration (available only for n ₃ n ₄ = 06 or 07) 013 = 12 V with 0.6 V droop load sharing function configuration (Vin 40-75, available only for n ₃ n ₄ = 06 or 07) 014 = 12.45 V with 0.6 V droop load sharing function configuration

 (Vin 40-75, available only for n₃n₄ = 06 or 07)

xxx = Application Specific Configuration

Packaging

20 converters/tray/box PE foam dissipative

Example: Product number BMR4532000/002 equals an Through hole mount lead length 3.69 mm (cut), open frame, digital interface with 9 V standard configuration variant.

Note 1: Surface mount option available for 8.1-13.2Vout open frame version. Can not be combined with base plate option.

For application specific configurations contact your local Ericsson Power Modules sales representative.

General Information
Reliability

The failure rate (λ) and mean time between failures (MTBF = $1/\lambda$) is calculated at max output power and an operating ambient temperature (T_A) of +40°C. Ericsson Power Modules uses Telcordia SR-332 Issue 2 Method 1 to calculate the mean steady-state failure rate and standard deviation (σ).

Telcordia SR-332 Issue 2 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

Mean steady-state failure rate, λ	Std. deviation, σ
403 nFailures/h	61 nFailures/h

MTBF (mean value) for the BMR453 series = 2.5 Mh.
MTBF at 90% confidence level = 2.1 Mh

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2002/95/EC and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Ericsson Power Modules products are found in the Statement of Compliance document.

Ericsson Power Modules fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals (REACH) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

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Input 36-75 V, Output up to 60 A / 396 W

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Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of the products.

Warranty

Warranty period and conditions are defined in Ericsson Power Modules General Terms and Conditions of Sale.

Limitation of Liability

Ericsson Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

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Safety Specification**General information**

Ericsson Power Modules DC/DC converters and DC/DC regulators are designed in accordance with safety standards IEC/EN/UL 60950-1 *Safety of Information Technology Equipment*.

IEC/EN/UL 60950-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Energy hazards
- Fire
- Mechanical and heat hazards
- Radiation hazards
- Chemical hazards

On-board DC/DC converters and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without "Conditions of Acceptability". Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use should comply with the requirements in IEC 60950-1, EN 60950-1 and UL 60950-1 *Safety of Information Technology Equipment*. There are other more product related standards, e.g. IEEE 802.3 CSMA/CD (Ethernet) Access Method, and ETS-300132-2 *Power supply interface at the input to telecommunications equipment, operated by direct current (dc)*, but all of these standards are based on IEC/EN/UL 60950-1 with regards to safety. Ericsson Power Modules DC/DC converters and DC/DC regulators are UL 60950-1 recognized and certified in accordance with EN 60950-1.

The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

The products should be installed in the end-use equipment, in accordance with the requirements of the ultimate application. Normally the output of the DC/DC converter is considered as SELV (Safety Extra Low Voltage) and the input source must be isolated by minimum Double or Reinforced Insulation from the primary circuit (AC mains) in accordance with IEC/EN/UL 60950-1.

Isolated DC/DC converters

It is recommended that a slow blow fuse is to be used at the input of each DC/DC converter. If an input filter is used in the circuit the fuse should be placed in front of the input filter.

In the rare event of a component problem that imposes a short circuit on the input source, this fuse will provide the following functions:

- Isolate the fault from the input power source so as not to affect the operation of other parts of the system.
- Protect the distribution wiring from excessive current and power loss thus preventing hazardous overheating.

The galvanic isolation is verified in an electric strength test. The test voltage (V_{iso}) between input and output is 1500 Vdc or 2250 Vdc (refer to product specification).

24 V DC systems

The input voltage to the DC/DC converter is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

48 and 60 V DC systems

If the input voltage to the DC/DC converter is 75 Vdc or less, then the output remains SELV (Safety Extra Low Voltage) under normal and abnormal operating conditions.

Single fault testing in the input power supply circuit should be performed with the DC/DC converter connected to demonstrate that the input voltage does not exceed 75 Vdc.

If the input power source circuit is a DC power system, the source may be treated as a TNV-2 circuit and testing has demonstrated compliance with SELV limits in accordance with IEC/EN/UL60950-1.

Non-isolated DC/DC regulators

The input voltage to the DC/DC regulator is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

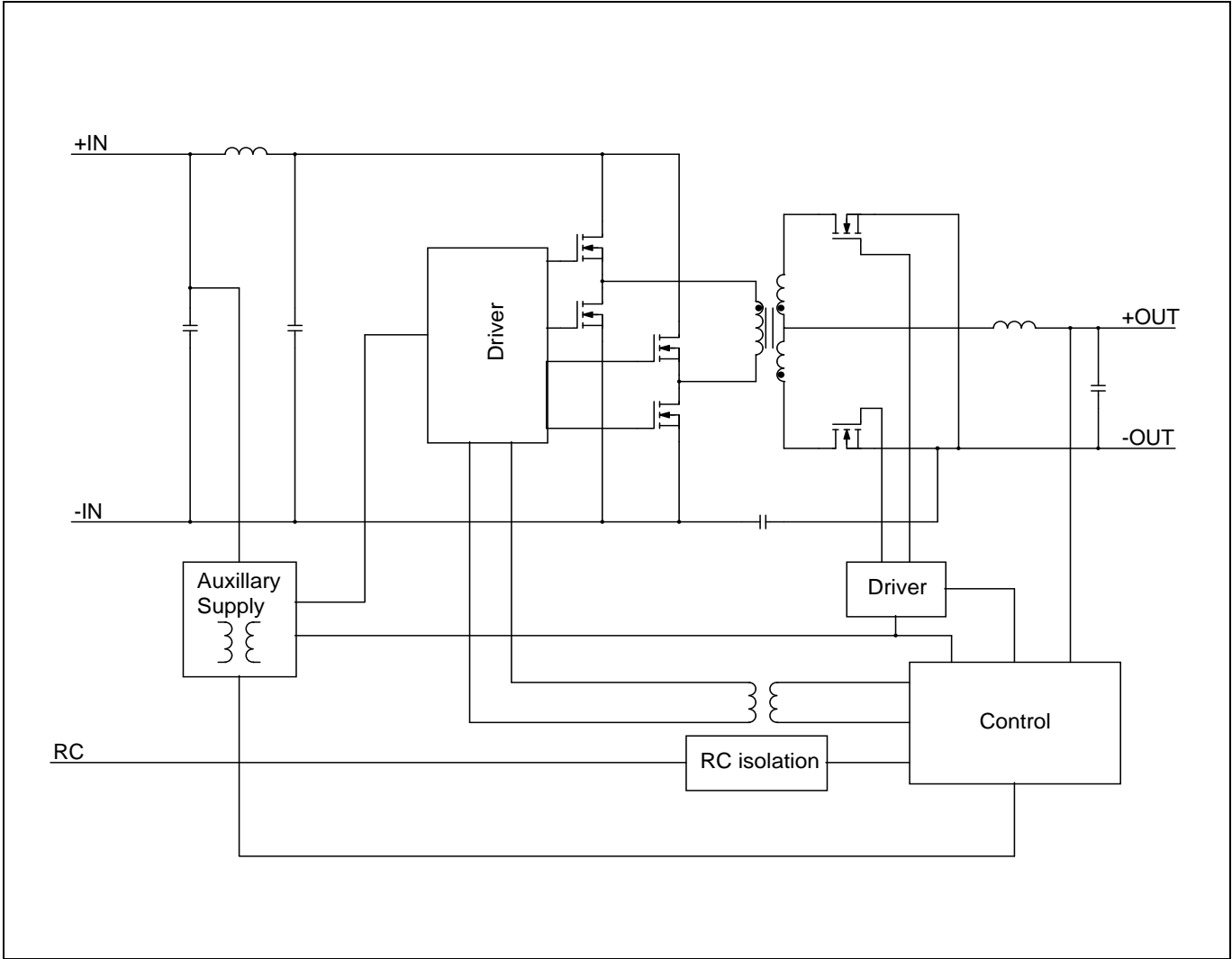
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Absolute Maximum Ratings

Characteristics		min	typ	max	Unit
T _{P1}	Operating Temperature (see Thermal Consideration section)	-40		+125	°C
T _S	Storage temperature	-55		+125	°C
V _I	Input voltage	-0.5		80	V
V _{iso}	Isolation voltage (input to output test voltage), see note 1			1500	Vdc
V _{tr}	Input voltage transient (Tp 100 ms)			100	V
V _{RC}	Remote Control pin voltage	-0.3		18	V
V Logic I/O	SALERT, CTRL, SYNC, SCL, SDA, SA(0,1)	-0.3		3.6	V

Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits of Output data or Electrical Characteristics. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.
Note 1: Isolation voltage (input/output to base-plate) max 750 Vdc.

Fundamental Circuit Diagram



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Functional Description
 $T_{P1} = -40$ to $+90^{\circ}\text{C}$, $V_I = 36$ to 75 V, sense pins connected to output pins unless otherwise specified under Conditions.

 Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, max I_O , unless otherwise specified under Conditions

Configuration File: 190 10-CDA 102 935/001 rev D

Characteristics		Conditions	min	typ	max	Unit
PMBus monitoring accuracy						
VIN_READ	Input voltage		-3	+0.4	3	%
VOUT_READ	Output voltage	$V_I = 53$ V	-1.0	-0.3	1.0	%
IOUT_READ	Output current	$V_I = 53$ V, 50-100% of max I_O	-6	-0.1	6	%
IOUT_READ	Output current	$V_I = 53$ V, 10% of max I_O	-0.7	-	0.7	A
TEMP_READ	Temperature		-5	-	5	$^{\circ}\text{C}$
Fault Protection Characteristics						
Input Under Voltage Lockout, UVLO	Factory default		-	33	-	V
	Setpoint accuracy		-3	-	3	%
	Hysteresis	Factory default	-	1.8	-	V
		Configurable via PMBus of threshold range, Note 1	0	-	-	V
	Delay		-	200	-	μs
(Output voltage) Over/Under Voltage Protection, OVP/UVF	VOUT_UV_FAULT_LIMIT	Factory default	-	0	-	V
		Configurable via PMBus, Note 1	0	-	16	V
	VOUT_OV_FAULT_LIMIT	Factory default	-	15.6	-	V
		Configurable via PMBus, Note 1	V_{OUT}	-	16	V
	fault response time		-	200	-	μs
Over Current Protection, OCP	Setpoint accuracy	I_O	-6	-	6	%
	IOUT_OC_FAULT_LIMIT	Factory default	-	38	-	A
		Configurable via PMBus, Note 1	0	-	100	
	fault response time		-	200	-	μs
Over Temperature Protection, OTP	OTP_FAULT_LIMIT	Factory default	-	135	-	$^{\circ}\text{C}$
		Configurable via PMBus, Note 1	-50	-	135	
	OTP hysteresis	Factory default	-	10	-	
		Configurable via PMBus, Note 1	0	-	165	
	fault response time		-	200	-	μs
Logic Input/Output Characteristics						
Logic input low (V_{IL})		CTRL_CS, SA0, SA1, PG_SYNC, SCL, SDA,	-	-	0.8	V
Logic input high (V_{IH})			2.0	-	-	V
Logic output low (V_{OL})		CTRL_CS, PG_SYNC, SALERT, SCL, SDA $I_{OL} = 5$ mA	-	-	0.4	V
Logic output high (V_{OH})		CTRL_CS, PG_SYNC, SALERT, SCL, SDA $I_{OH} = -5$ mA	2.8	-	-	V
Setup time, SMBus			100	-	-	ns
Hold time, SMBus			300	-	-	ns
Bus free time T(BUF)		Note 2	200	-	-	us

Note 1: See Operating Information section.

Note 2: It is recommended that a PMBus master read back written data for verification i.e. do not rely on the ACK/NACK bit since this bit are as susceptible to errors as any other bit*. However, under very rare operating conditions, it is possible to get intermittent read back failures. It is therefore recommended to implement error handling in the master that also deals with those situations.

BMR 453 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 60 A / 396 W

EN/LZT 146 395 R6A July 2011

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3.3V, 60A / 198W Electrical Specification
BMR 453 0002/003
 $T_{P1} = -40$ to $+90^{\circ}\text{C}$, $V_I = 36$ to 75 V, sense pins connected to output pins unless otherwise specified under Conditions.

 Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, max I_O , unless otherwise specified under Conditions.

 Additional $C_{out} = 0.1$ mF, Configuration File: 190 10-CDA 102 935/003 rev B

Characteristics		Conditions	min	typ	max	Unit
V _I	Input voltage range		36		75	V
V _{Ioff}	Turn-off input voltage	Decreasing input voltage	32	33	34	V
V _{Ion}	Turn-on input voltage	Increasing input voltage	34	35	36	V
C _I	Internal input capacitance			10		μF
P _O	Output power		0		198	W
η	Efficiency	50% of max I _O		94.7		%
		max I _O		93.3		
		50% of max I _O , V _I = 48 V		94.9		
		max I _O , V _I = 48 V		93.3		
P _d	Power Dissipation	max I _O		14.1	20.8	W
P _{li}	Input idling power	I _O = 0 A, V _I = 53 V		1.7		W
P _{RC}	Input standby power	V _I = 53 V (turned off with RC)		123		mW
f _s	Default switching frequency	0-100% of max I _O see Note 1	171	180	189	kHz

V_{Oi}	Output voltage initial setting and accuracy	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, $I_O = 60$ A	3.26	3.3	3.36	V
V_O	Output adjust range	See operating information	3.0		6.7	V
	Output voltage tolerance band	0-100% of max I_O	3.22		3.38	V
	Line regulation	max I_O		4	16	mV
	Load regulation	$V_I = 53$ V, 1-100% of max I_O		4	12	mV
V_{tr}	Load transient voltage deviation	$V_I = 53$ V, Load step 25-75-25% of max I_O , $di/dt = 1$ A/ μs , see Note 2		± 0.2		V
t_{tr}	Load transient recovery time			250		μs
t_r	Ramp-up time (from 10-90% of V_{Oi})	10-100% of max I_O , $T_{P1} = 25^{\circ}\text{C}$, $V_I = 53$ V		8		ms
t_s	Start-up time (from V_I connection to 90% of V_{Oi})	see Note 3		140		ms
t_f	Vin shutdown fall time (from V_I off to 10% of V_O)	max I_O		0.2		ms
		$I_O = 0$ A		4.5		s
t_{RC}	RC start-up time	max I_O		52		ms
		max I_O		3		ms
	RC shutdown fall time (from RC off to 10% of V_O)	$I_O = 0$ A		4.5		s
I_O	Output current		0		60	A
I_{lim}	Current limit threshold	$V_O = 3.0$ V, $T_{P1} < \text{max } T_{P1}$	61	66	82	A
I_{sc}	Short circuit current	$T_{P1} = 25^{\circ}\text{C}$, $V_O < 0.2$ V, see Note 4		11		A
C_{out}	Recommended Capacitive Load	$T_{P1} = 25^{\circ}\text{C}$, see Note 5	0.1	6	10	mF
V_{Oac}	Output ripple & noise	See ripple & noise section, max I_O , V_{Oi}		30	100	mVp-p
OVP	Over voltage protection	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, 10-100% of max I_O , see Note 6		4.6		V

Note 1: Frequency may be adjusted via PMBus, see Operating Information section.

 Note 2: $C_{out} = 6$ mF used at load transient test.

Note 3: Start-up and Ramp-up time can be increased via PMBus, see Operation Information section.

Note 4: RMS current in hiccup mode.

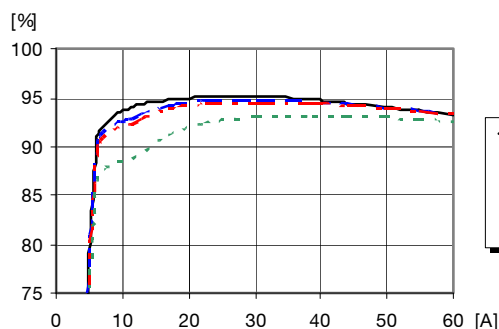
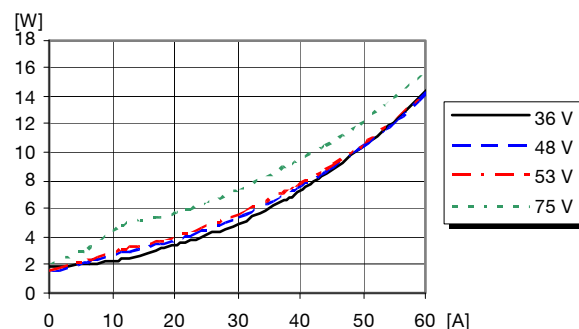
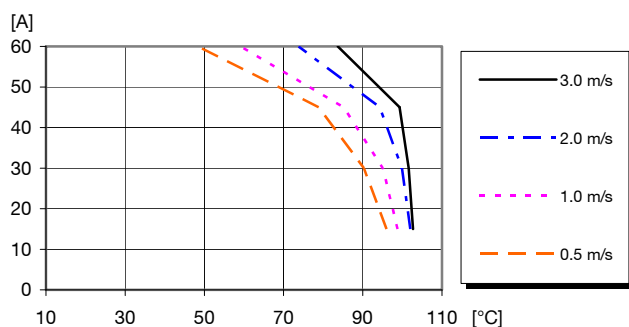
Note 5: Low ESR-value.

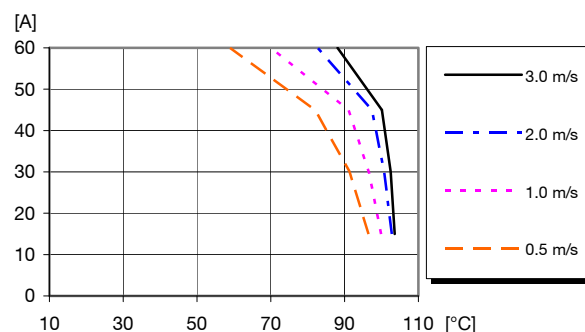
Note 6: OVP-level can be adjusted via PMBus, see Operation Information.

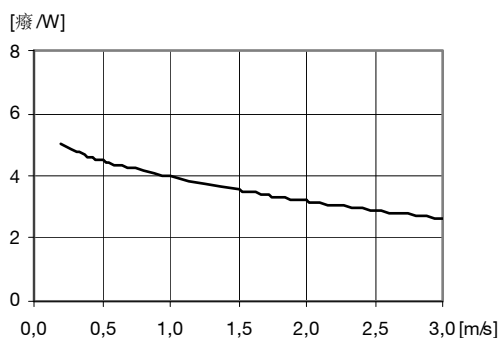
BMR 453 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 60 A / 396 W

EN/LZT 146 395 R6A July 2011

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3.3V, 60A / 198W Electrical Specification
BMR 453 0002/003
Efficiency

 Efficiency vs. load current and input voltage at $T_{P1} = +25^{\circ}\text{C}$
Power Dissipation

 Dissipated power vs. load current and input voltage at $T_{P1} = +25^{\circ}\text{C}$
Output Current Derating, open frame

 Available load current vs. ambient air temperature and airflow at $V_I = 53\text{ V}$. See Thermal Consideration section.

Output Current Derating, base plate option

 Available load current vs. ambient air temperature and airflow at $V_I = 53\text{ V}$. See Thermal Consideration section.

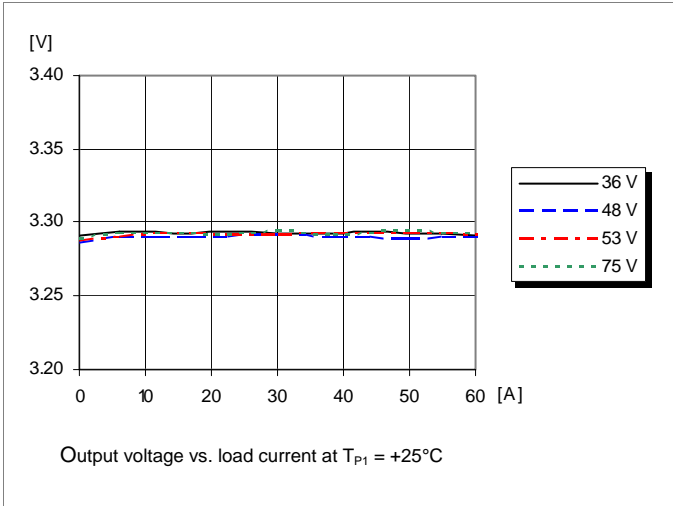
Thermal Resistance, base plate option

 Thermal resistance vs. airspeed measured at the converter. Tested in wind tunnel with airflow and test conditions as per the Thermal consideration section. $V_I = 53\text{ V}$

BMR 453 series Fully regulated Intermediate Bus Converters Input 36-75 V, Output up to 60 A / 396 W	EN/LZT 146 395 R6A July 2011
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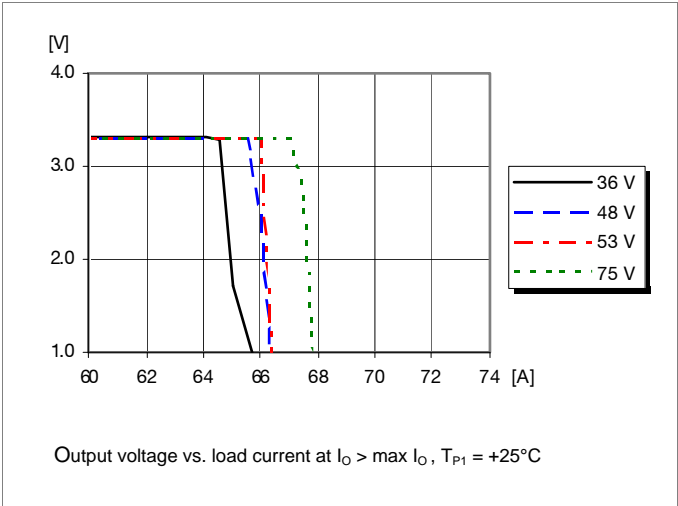
3.3V, 60A / 198W Electrical Specification

BMR 453 0002/003

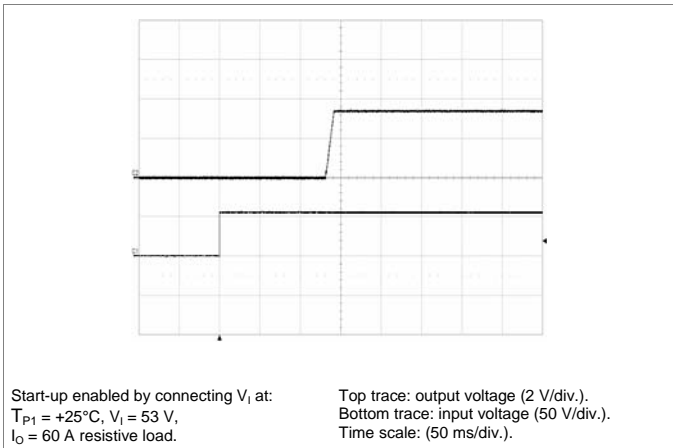
Output Characteristics



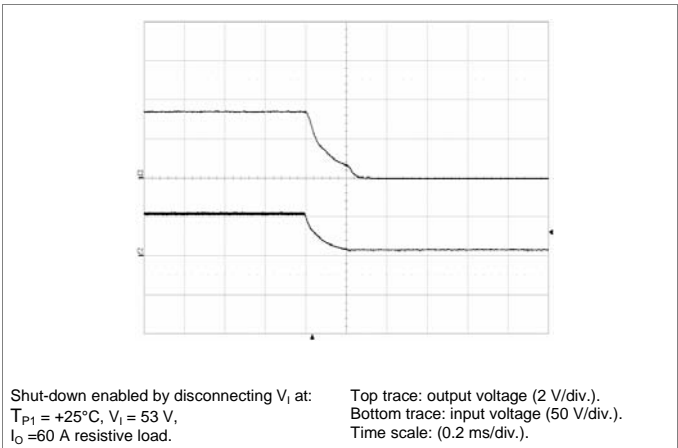
Current Limit Characteristics



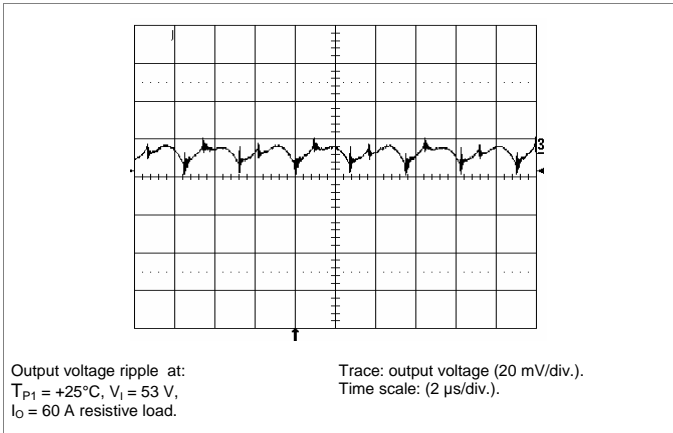
Start-up



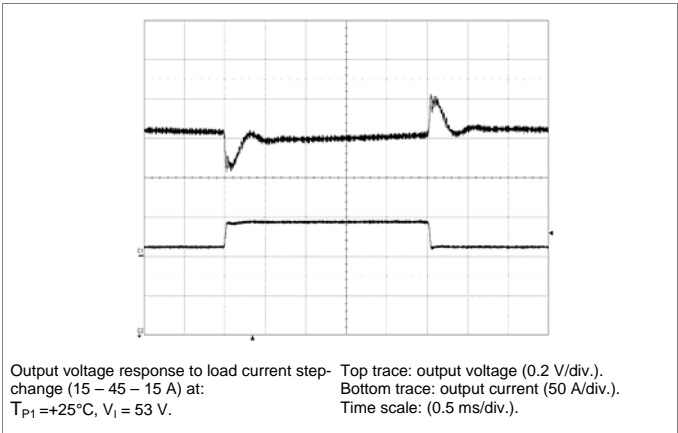
Shut-down



Output Ripple & Noise



Output Load Transient Response



BMR 453 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 60 A / 396 W

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5.0V, 60A / 300W Electrical Specification
BMR 453 0002/004
 $T_{P1} = -40$ to $+90^{\circ}\text{C}$, $V_I = 36$ to 75 V, sense pins connected to output pins unless otherwise specified under Conditions.

 Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, max I_O , unless otherwise specified under Conditions.

 Additional $C_{out} = 0.1$ mF, Configuration File: 190 10-CDA 102 935/004 rev B

Characteristics		Conditions	min	typ	max	Unit
V _I	Input voltage range		36		75	V
V _{Ioff}	Turn-off input voltage	Decreasing input voltage	32	33	34	V
V _{Ion}	Turn-on input voltage	Increasing input voltage	34	35	36	V
C _I	Internal input capacitance			10		μF
P _O	Output power		0		300	W
η	Efficiency	50% of max I _O		96.0		%
		max I _O		94.8		
		50% of max I _O , V _I = 48 V		96.1		
		max I _O , V _I = 48 V		94.8		
P _d	Power Dissipation	max I _O		16.5	22.8	W
P _{li}	Input idling power	I _O = 0 A, V _I = 53 V		1.9		W
P _{RC}	Input standby power	V _I = 53 V (turned off with RC)		143		mW
f _s	Default switching frequency	0-100% of max I _O see Note 1	171	180	189	kHz

V_{Oi}	Output voltage initial setting and accuracy	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, $I_O = 60$ A	4.95	5.0	5.05	V
V_O	Output adjust range	See operating information	3.0		6.7	V
	Output voltage tolerance band	0-100% of max I_O	4.9		5.1	V
	Line regulation	max I_O		3	19	mV
	Load regulation	$V_I = 53$ V, 1-100% of max I_O		6	12	mV
V_{tr}	Load transient voltage deviation	$V_I = 53$ V, Load step 25-75-25% of max I_O , $di/dt = 1$ A/ μs , see Note 2		± 0.2		V
t_{tr}	Load transient recovery time			200		μs
t_r	Ramp-up time (from 10-90% of V_{Oi})	10-100% of max I_O , $T_{P1} = 25^{\circ}\text{C}$, $V_I = 53$ V		8		ms
t_s	Start-up time (from V_I connection to 90% of V_{Oi})	see Note 3		140		ms
t_f	Vin shutdown fall time (from V_I off to 10% of V_O)	max I_O		0.2		ms
		$I_O = 0$ A		4.5		s
	RC start-up time	max I_O		53		ms
t_{RC}	RC shutdown fall time (from RC off to 10% of V_O)	max I_O		2		ms
		$I_O = 0$ A		4.5		s
I_O	Output current		0		60	A
I_{lim}	Current limit threshold	$V_O = 4.5$ V, $T_{P1} < \text{max } T_{P1}$	61	66	82	A
I_{sc}	Short circuit current	$T_{P1} = 25^{\circ}\text{C}$, $V_O < 0.2$ V, see Note 4		11		A
C_{out}	Recommended Capacitive Load	$T_{P1} = 25^{\circ}\text{C}$, see Note 5	0.1	6	10	mF
V_{Oac}	Output ripple & noise	See ripple & noise section, max I_O , V_{Oi}		25	100	mVp-p
OVP	Over voltage protection	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, 10-100% of max I_O , see Note 6		6.8		V

Note 1: Frequency may be adjusted via PMBus, see Operating Information section.

 Note 2: $C_{out} = 6$ mF used at load transient test.

Note 3: Start-up and Ramp-up time can be increased via PMBus, see Operation Information section.

Note 4: RMS current in hiccup mode.

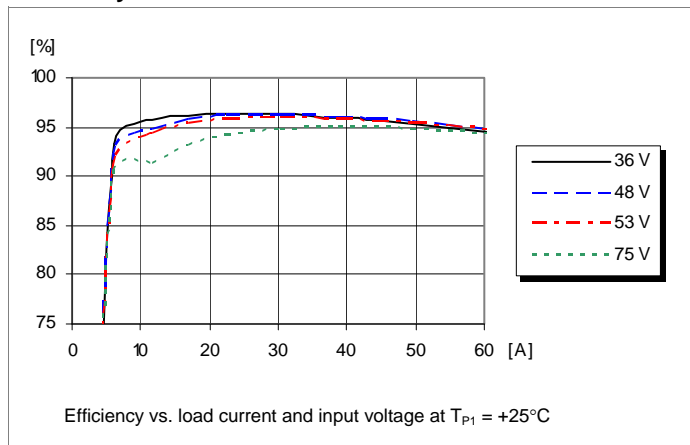
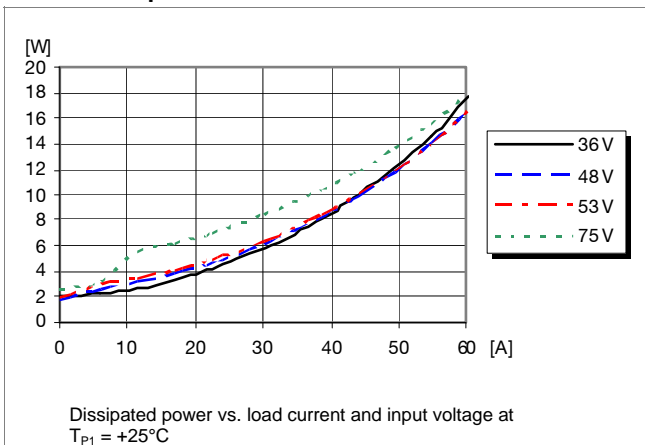
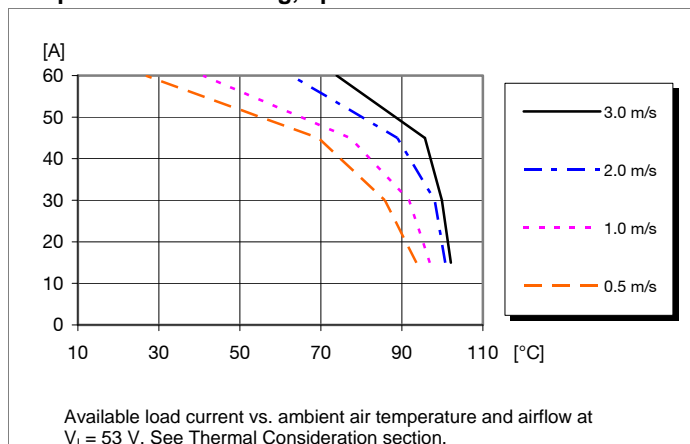
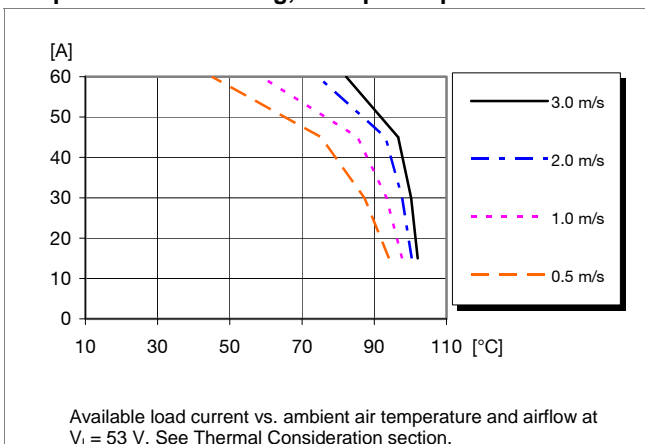
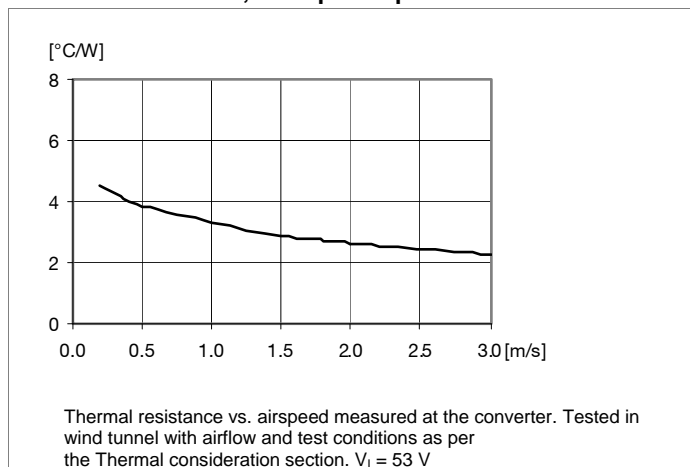
Note 5: Low ESR-value.

Note 6: OVP-level can be adjusted via PMBus, see Operation Information.

BMR 453 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 60 A / 396 W

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5.0V, 60A / 300W Electrical Specification
BMR 453 0002/004
Efficiency

Power Dissipation

Output Current Derating, open frame

Output Current Derating, base plate option

Thermal Resistance, base plate option


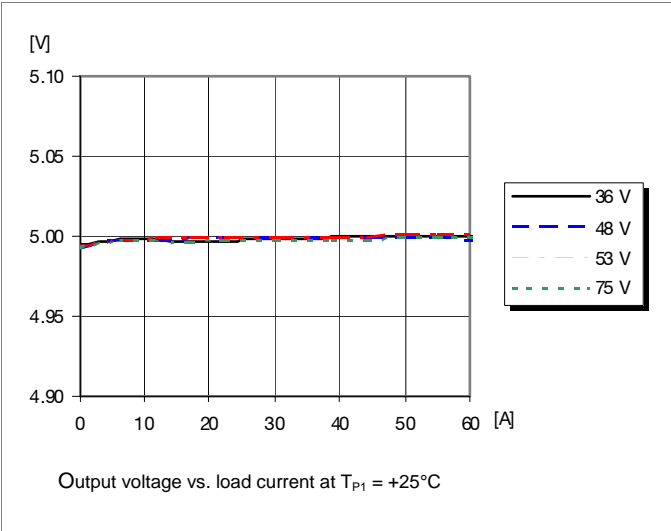
BMR 453 series Fully regulated Intermediate Bus Converters
Input 36-75 V, Output up to 60 A / 396 W

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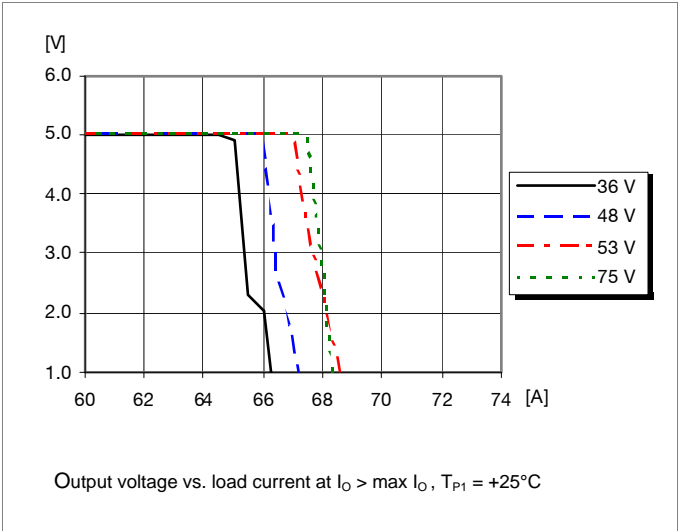
5.0V, 60A / 300W Electrical Specification

BMR 453 0002/004

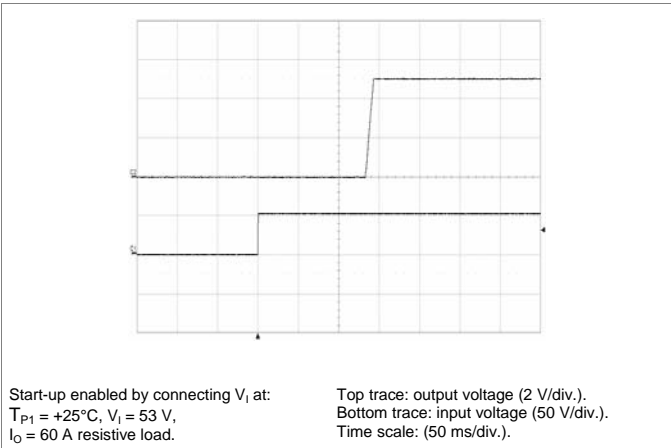
Output Characteristics



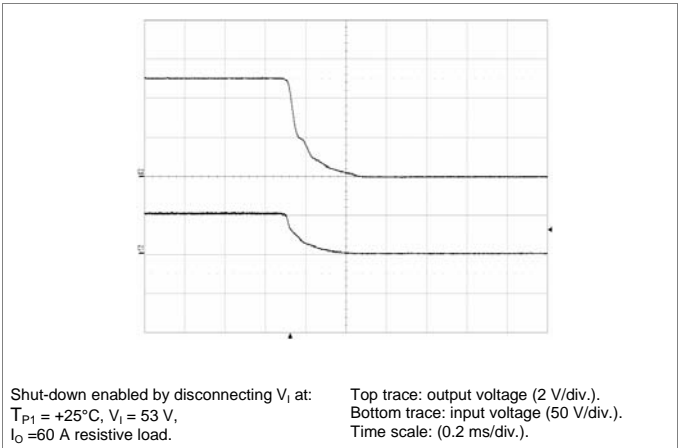
Current Limit Characteristics



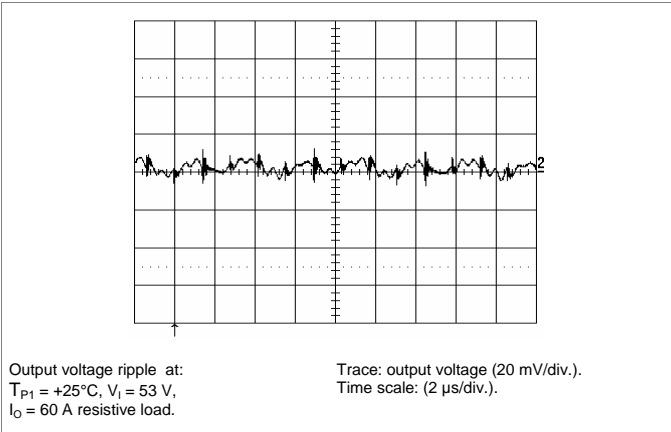
Start-up



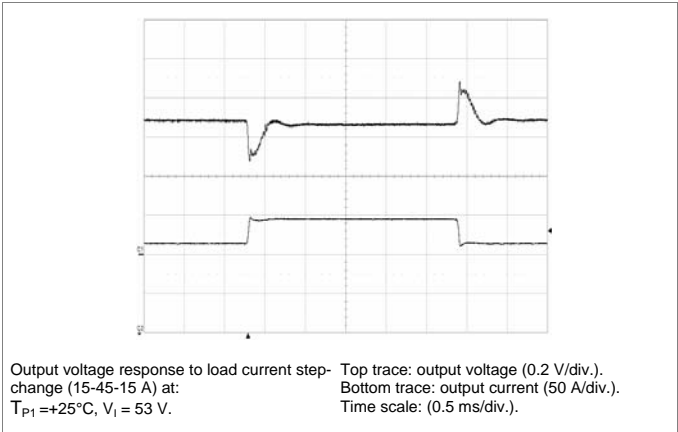
Shut-down



Output Ripple & Noise



Output Load Transient Response



BMR 453 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 60 A / 396 W

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9.0V, 33A / 297W Electrical Specification
BMR 453 0000/002
 $T_{P1} = -40$ to $+90^{\circ}\text{C}$, $V_I = 36$ to 75 V, sense pins connected to output pins unless otherwise specified under Conditions.

 Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, max I_O , unless otherwise specified under Conditions.

 Additional $C_{out} = 0.1$ mF, Configuration File: 190 10-CDA 102 935/002 rev D

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage range		36		75	V
V_{loff}	Turn-off input voltage	Decreasing input voltage	32	33	34	V
V_{lon}	Turn-on input voltage	Increasing input voltage	34	35	36	V
C_I	Internal input capacitance			18		μF
P_O	Output power		0		297	W
η	Efficiency	50% of max I_O		96		%
		max I_O		95		
		50% of max I_O , $V_I = 48$ V		96		
		max I_O , $V_I = 48$ V		95		
P_d	Power Dissipation	max I_O		15.5	24.7	W
P_{li}	Input idling power	$I_O = 0$ A, $V_I = 53$ V		2.1		W
P_{RC}	Input standby power	$V_I = 53$ V (turned off with RC)		190		mW
f_s	Default switching frequency	0-100% of max I_O see Note 1	133	140	145	kHz

V_{Oi}	Output voltage initial setting and accuracy	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, $I_O = 17$ A	8.90	9.0	9.10	V
V_O	Output adjust range	See operating information	8.1		13.2	V
	Output voltage tolerance band	0-100% of max I_O	8.82		9.18	V
	Line regulation	max I_O		15	50	mV
	Load regulation	$V_I = 53$ V, 1-100% of max I_O		60	85	mV
V_{tr}	Load transient voltage deviation	$V_I = 53$ V, Load step 25-75-25% of max I_O , $di/dt = 1$ A/ μs , see Note 2		± 0.3		V
t_{tr}	Load transient recovery time			250		μs
t_r	Ramp-up time (from 10-90% of V_{Oi})	10-100% of max I_O , $T_{P1} = 25^{\circ}\text{C}$, $V_I = 53$ V		8		ms
t_s	Start-up time (from V_I connection to 90% of V_{Oi})	see Note 3		140		ms
t_f	Vin shutdown fall time (from V_I off to 10% of V_O)	max I_O		0.4		ms
		$I_O = 0$ A		8		s
t_{RC}	RC start-up time	max I_O		53		ms
		max I_O		3.2		ms
		$I_O = 0$ A		8		s
I_O	Output current		0		33	A
I_{lim}	Current limit threshold	$V_O = 8.1$ V, $T_{P1} < \text{max } T_{P1}$	34	38	43	A
I_{sc}	Short circuit current	$T_{P1} = 25^{\circ}\text{C}$, $V_O < 0.2$ V, see Note 4		6		A
C_{out}	Recommended Capacitive Load	$T_{P1} = 25^{\circ}\text{C}$, see Note 5	0.1	3.3	6	mF
V_{Oac}	Output ripple & noise	See ripple & noise section, max I_O , V_{Oi}		50	120	mVp-p
OVP	Over voltage protection	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, 10-100% of max I_O , see Note 6		15.6		V

Note 1: Frequency may be adjusted via PMBus, see Operating Information section.

 Note 2: $C_{out} = 3.3$ mF used at load transient test.

Note 3: Start-up and Ramp-up time can be increased via PMBus, see Operation Information section.

Note 4: RMS current in hiccup mode.

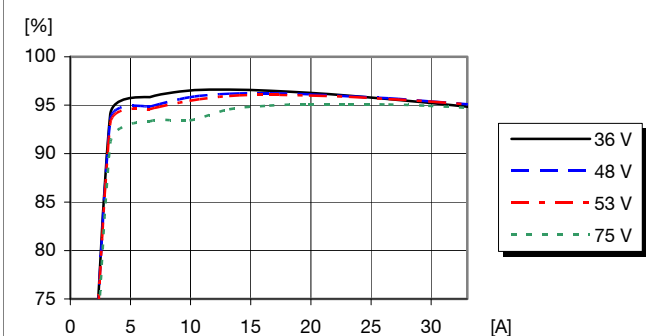
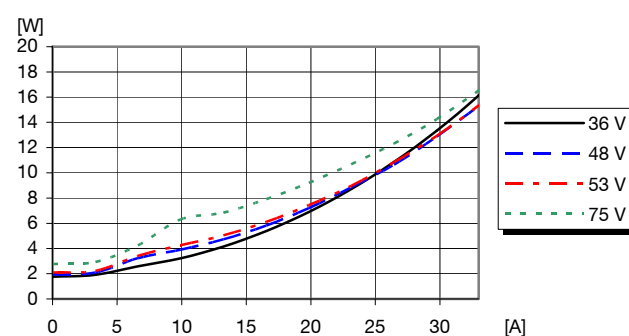
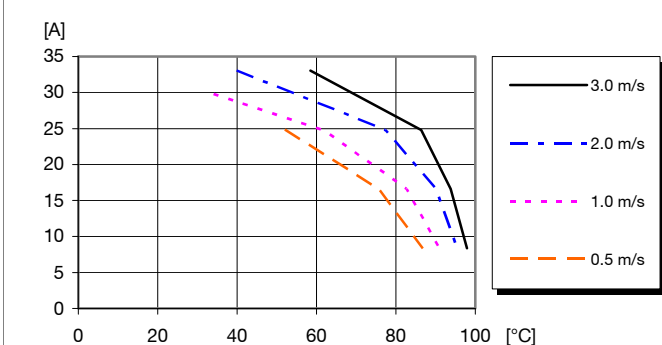
Note 5: Low ESR-value.

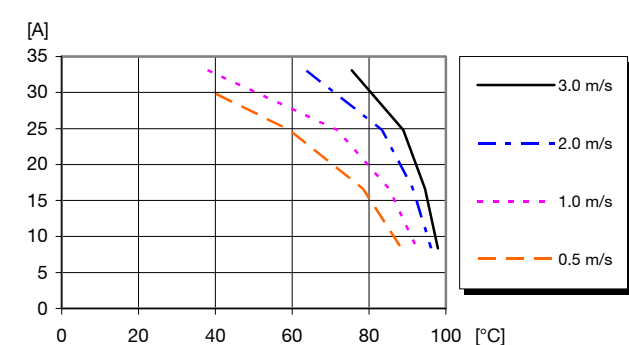
Note 6: OVP-level can be adjusted via PMBus, see Operation Information.

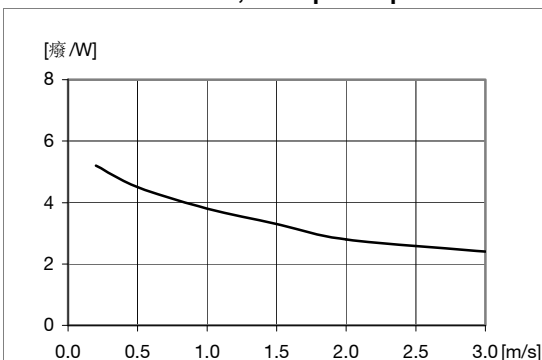
BMR 453 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 60 A / 396 W

EN/LZT 146 395 R6A July 2011

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9.0V, 33A / 297W Electrical Specification
BMR 453 0000/002
Efficiency

 Efficiency vs. load current and input voltage at $T_{P1} = +25^{\circ}\text{C}$
Power Dissipation

 Dissipated power vs. load current and input voltage at $T_{P1} = +25^{\circ}\text{C}$
Output Current Derating, open frame

 Available load current vs. ambient air temperature and airflow at $V_I = 53\text{ V}$. See Thermal Consideration section.

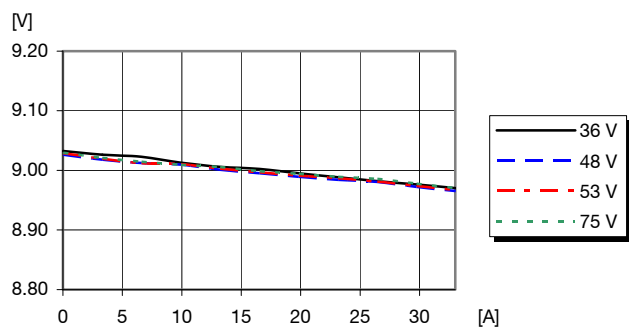
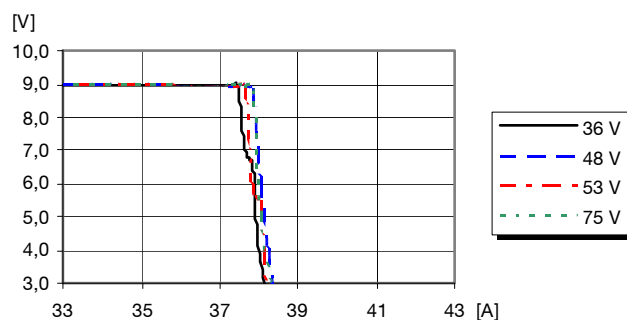
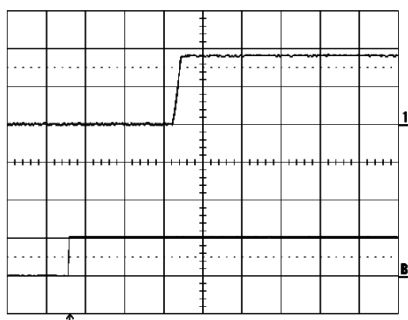
Output Current Derating, base plate option

 Available load current vs. ambient air temperature and airflow at $V_I = 53\text{ V}$. See Thermal Consideration section.

Thermal Resistance, base plate option

 Thermal resistance vs. airspeed measured at the converter. Tested in wind tunnel with airflow and test conditions as per the Thermal consideration section. $V_I = 53\text{ V}$

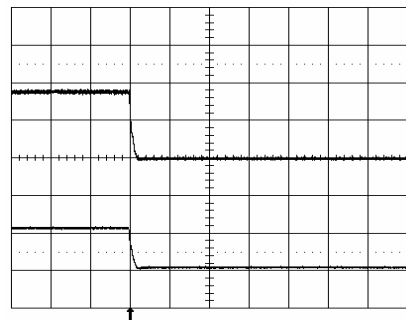
BMR 453 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 60 A / 396 W

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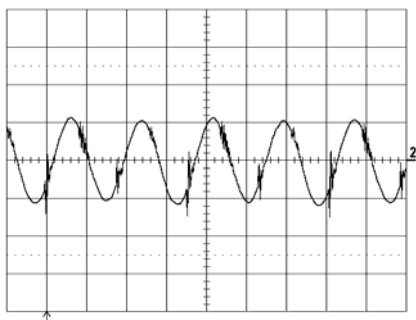
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9.0V, 33A / 297W Electrical Specification
BMR 453 0000/002
Output Characteristics

 Output voltage vs. load current at $T_{P1} = +25^{\circ}\text{C}$
Current Limit Characteristics

 Output voltage vs. load current at $I_O > \max I_O$, $T_{P1} = +25^{\circ}\text{C}$
Start-up

 Start-up enabled by connecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 33\text{ A}$ resistive load.

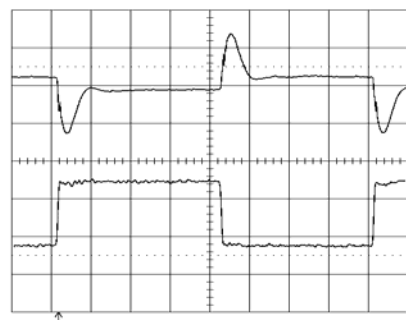
 Top trace: output voltage (5 V/div.).
 Bottom trace: input voltage (50 V/div.).
 Time scale: (50 ms/div.).

Shut-down

 Shut-down enabled by disconnecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 33\text{ A}$ resistive load.

 Top trace: output voltage (2 V/div.).
 Bottom trace: input voltage (50 V/div.).
 Time scale: (0.2 ms/div.).

Output Ripple & Noise

 Output voltage ripple at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 33\text{ A}$ resistive load.

 Trace: output voltage (20 mV/div.).
 Time scale: (2 μs /div.).

Output Load Transient Response

 Output voltage response to load current step-
 change (8.25-24.75-8.25 A) at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$.

 Top trace: output voltage (0.2 V/div.).
 Bottom trace: output current (10 A/div.).
 Time scale: (0.5 ms/div.).

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12.0V, 33A / 396W Electrical Specification
BMR 453 0000/001
 $T_{P1} = -40$ to $+90^{\circ}\text{C}$, $V_I = 40$ to 75 V, sense pins connected to output pins unless otherwise specified under Conditions.

 Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, max I_O , unless otherwise specified under Conditions.

 Additional $C_{out} = 0.1$ mF, Configuration File: 190 10-CDA 102 935/001 rev D

Characteristics		Conditions	min	typ	max	Unit
V _I	Input voltage range		40		75	V
V _{Ioff}	Turn-off input voltage	Decreasing input voltage	32	33	34	V
V _{Ion}	Turn-on input voltage	Increasing input voltage	34	35	36	V
C _I	Internal input capacitance			18		μF
P _O	Output power		0		396	W
η	Efficiency	50% of max I _O		96.5		%
		max I _O		95.5		
		50% of max I _O , V _I = 48 V		96.5		
		max I _O , V _I = 48 V		95.5		
P _d	Power Dissipation	max I _O		18.3	27.1	W
P _{ii}	Input idling power	I _O = 0 A, V _I = 53 V		2.4		W
P _{RC}	Input standby power	V _I = 53 V (turned off with RC)		190		mW
f _s	Default switching frequency	0-100% of max I _O see Note 1	133	140	145	kHz

V_{Oi}	Output voltage initial setting and accuracy	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, $I_O = 17$ A	11.88	12.0	12.12	V
V_O	Output adjust range	See operating information	8.1		13.2	V
	Output voltage tolerance band	0-100% of max I_O	11.76		12.24	V
	Line regulation	max I_O		20	60	mV
	Load regulation	$V_I = 53$ V, 1-100% of max I_O		60	90	mV
V_{tr}	Load transient voltage deviation	$V_I = 53$ V, Load step 25-75-25 % of max I_O , $di/dt = 1$ A/ μs , see Note 2		± 0.4		V
t_{tr}	Load transient recovery time			250		μs
t_r	Ramp-up time (from 10-90% of V_{Oi})	10-100% of max I_O , $T_{P1} = 25^{\circ}\text{C}$, $V_I = 53$ V		8		ms
t_s	Start-up time (from V_I connection to 90% of V_{Oi})	see Note 3		140		ms
t_f	Vin shutdown fall time (from V_I off to 10% of V_O)	max I_O		0.4		ms
		$I_O = 0$ A		7		s
t_{RC}	RC start-up time	max I_O		53		ms
		max I_O		3.2		ms
	RC shutdown fall time (from RC off to 10% of V_O)	$I_O = 0$ A		7		s
I_O	Output current		0		33	A
I_{lim}	Current limit threshold	$V_O = 10.8$ V, $T_{P1} < \max T_{ref}$	34	38	43	A
I_{sc}	Short circuit current	$T_{P1} = 25^{\circ}\text{C}$, see Note 4		-		A
C_{out}	Recommended Capacitive Load	$T_{P1} = 25^{\circ}\text{C}$, see Note 5	0.1	3.3	6	mF
V_{Oac}	Output ripple & noise	See ripple & noise section, max I_O		60	120	mVp-p
OVP	Over voltage protection	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, 10-100% of max I_O , see Note 6		15.6		V

Note 1: Frequency may be adjusted with PMBus communication. See Operating Information section

 Note 2: $C_{out} = 3.3$ mF used at load transient test.

Note 3: Start-up and Ramp-up time can be increased via PMBus, see Operation Information section.

Note 4: OCP in latch mode

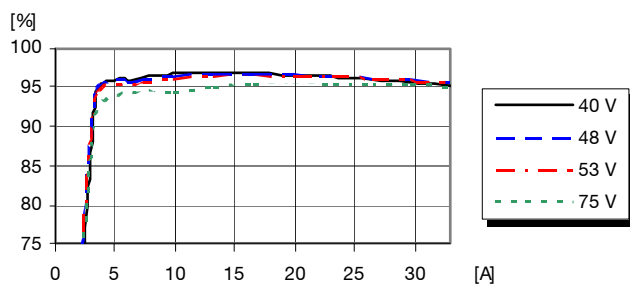
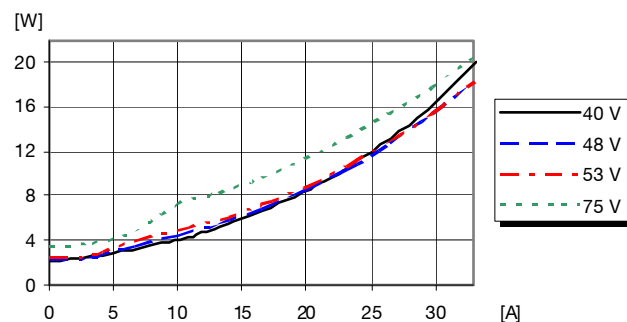
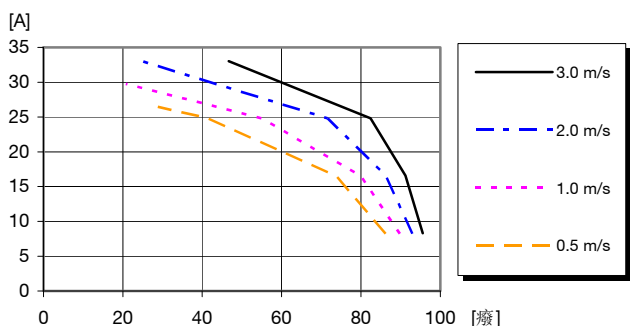
Note 5: Low ESR-value

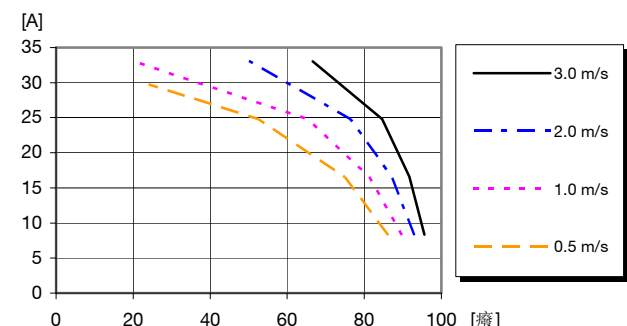
Note 6: OVP-level can be adjusted via PMBus, see Operation Information.

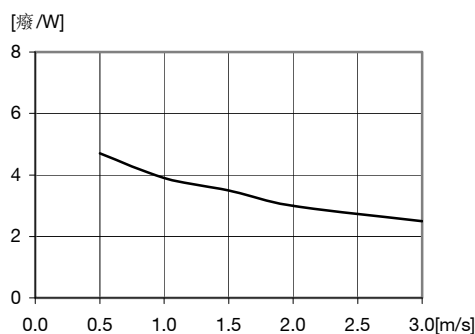
BMR 453 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 60 A / 396 W

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12.0V, 33A / 396W Electrical Specification
BMR 453 0000/001
Efficiency

 Efficiency vs. load current and input voltage at $T_{P1} = +25^{\circ}\text{C}$
Power Dissipation

 Dissipated power vs. load current and input voltage at $T_{P1} = +25^{\circ}\text{C}$
Output Current Derating, open frame

 Available load current vs. ambient air temperature and airflow at $V_i = 53\text{ V}$. See Thermal Consideration section.

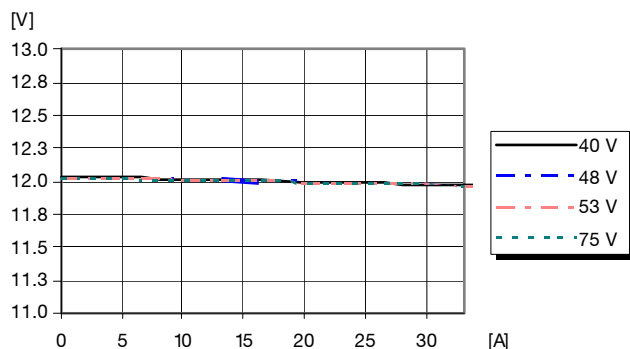
Output Current Derating, base plate option

 Available load current vs. ambient air temperature and airflow at $V_i = 53\text{ V}$. See Thermal Consideration section.

Thermal Resistance, base plate option

 Thermal resistance vs. airspeed measured at the converter. Tested in wind tunnel with airflow and test conditions as per the Thermal consideration section. $V_i = 53\text{ V}$, $I_o = 25\text{ A}$

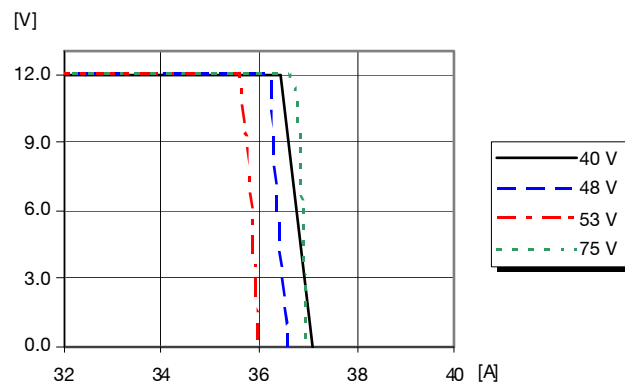
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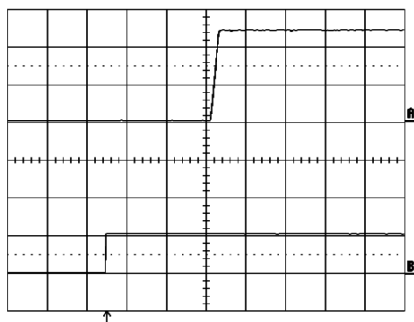
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12.0V, 33A / 396W Electrical Specification
BMR 453 0000/001
Output Characteristics


Output voltage vs. load current at $T_{P1} = +25^{\circ}\text{C}$
 The output voltage range is limited at 36V input voltage.

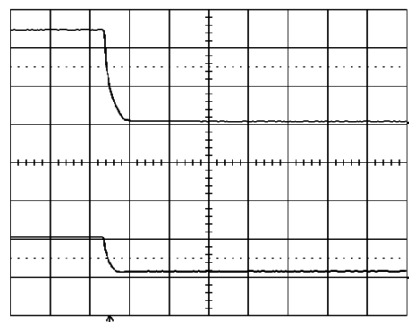
Current Limit Characteristics


Output voltage vs. load current at $I_O > \max I_O$, $T_{P1} = +25^{\circ}\text{C}$

Start-up


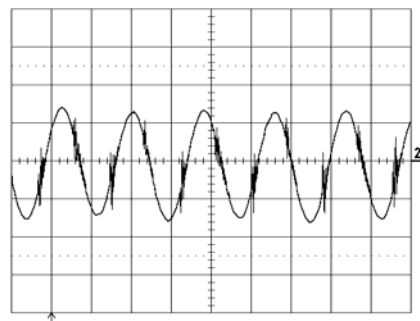
Start-up enabled by connecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53 \text{ V}$,
 $I_O = 33 \text{ A}$ resistive load.

Top trace: output voltage (5 V/div.).
 Bottom trace: input voltage (50 V/div.).
 Time scale: (50 ms/div.).

Shut-down


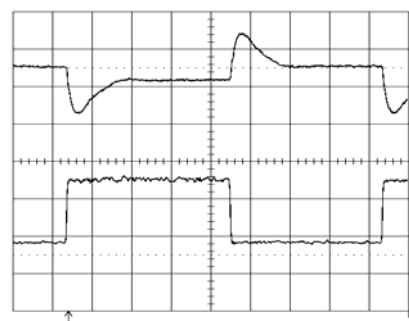
Shut-down enabled by disconnecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53 \text{ V}$,
 $I_O = 33 \text{ A}$ resistive load.

Top trace: output voltage (5 V/div.).
 Bottom trace: input voltage (50 V/div.).
 Time scale: (1 ms/div.).

Output Ripple & Noise


Output voltage ripple at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53 \text{ V}$,
 $I_O = 33 \text{ A}$ resistive load.

Trace: output voltage (20 mV/div.).
 Time scale: (2 μs /div.).

Output Load Transient Response


Output voltage response to load current
 step-change (8.25-24.75-8.25 A) at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53 \text{ V}$, $C_O = 3.3\text{mF}$.

Top trace: output voltage (0.2 V/div.).
 Bottom trace: output current (10 A/div.).
 Time scale: (0.5 ms/div.).

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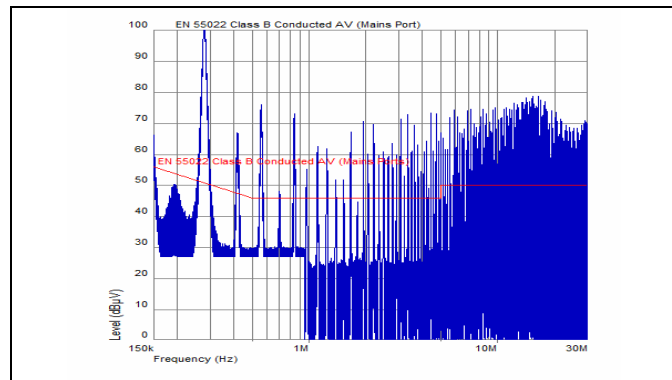
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EMC Specification

Conducted EMI measured according to EN55022, CISPR 22 and FCC part 15J (see test set-up). See Design Note 009 for further information. The fundamental switching frequency is 140 kHz for BMR 453 @ $V_I = 53$ V, max I_O .

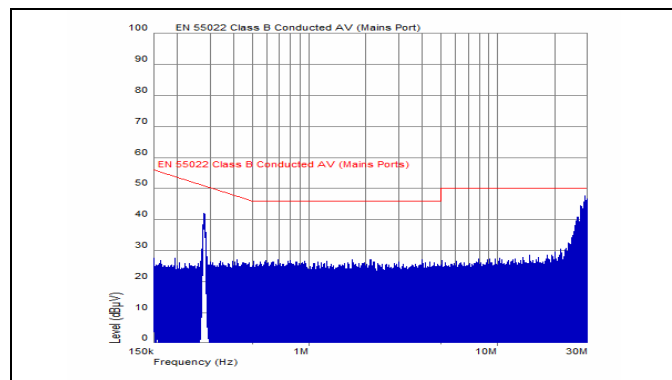
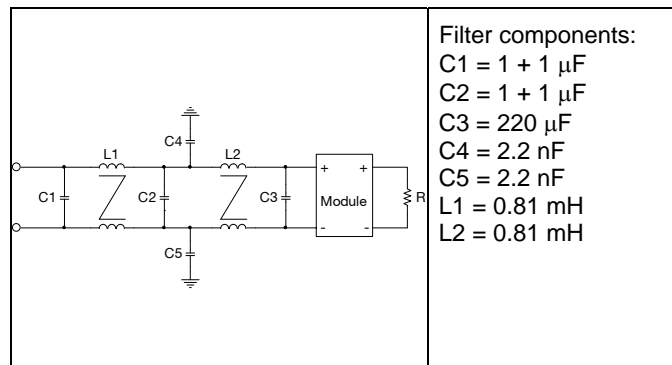
Conducted EMI Input terminal value (typ)



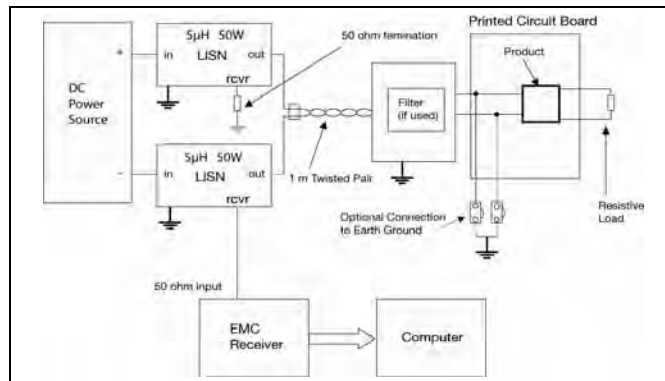
EMI without filter

External filter (class B)

Suggested external input filter in order to meet class B in EN 55022, CISPR 22 and FCC part 15J.



EMI with filter



Test set-up

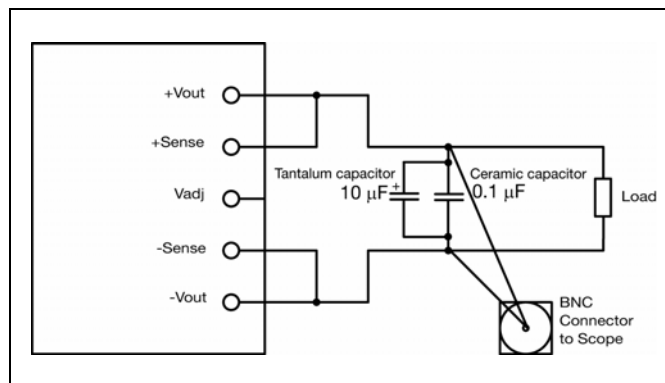
Layout recommendation

The radiated EMI performance of the product will depend on the PWB layout and ground layer design. It is also important to consider the stand-off of the product. If a ground layer is used, it should be connected to one of the output terminals and the equipment ground or chassis.

A ground layer will increase the stray capacitance in the PWB and improve the high frequency EMC performance.

Output ripple and noise

Output ripple and noise measured according to figure below. See Design Note 022 for detailed information.



Output ripple and noise test setup

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Operating information

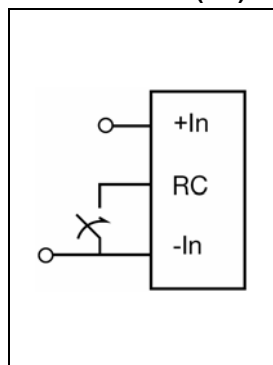
Input Voltage

The input voltage range 36 to 75 Vdc meets the requirements of the European Telecom Standard ETS 300 132-2 for normal input voltage range in -48 and -60 Vdc systems, -40.5 to -57.0 V and -50.0 to -72 V respectively. At input voltages exceeding 75 V, the power loss will be higher than at normal input voltage and T_{P1} must be limited to absolute max +125°C. The absolute maximum continuous input voltage is 80 Vdc.

Turn-off Input Voltage

The product monitors the input voltage and will turn on and turn off at predetermined levels. The turn on and turn off level and the hysteresis in between can be configured via the PMBus. The default hysteresis between turn on and turn off input voltage is set to 2 V.

Remote Control (RC)



The products are fitted with a configurable remote control function. The primary remote control is referenced to the primary negative input connection (-In). The RC function allows the converter to be turned on/off by an external device like a semiconductor or mechanical switch. The RC pin has an internal pull up resistor. The remote control functions can also be configured using the PMBus.

The device should be capable of sinking 0.7 mA. When the RC pin is left open, the voltage generated on the RC pin is max 6 V. The standard product is provided with "negative logic" remote control and will be off until the RC pin is connected to the -In. To turn on the product the voltage between RC pin and -In should be less than 1 V. To turn off the product the RC pin should be left open. In situations where it is desired to have the product to power up automatically without the need for control signals or a switch, the RC pin can be wired directly to -In. The logic option for the primary remote control is configured using the PMBus.

Remote Control (secondary side)

The CTRL CS pin can be configured as remote control via the PMBus interface. In the default configuration the CTRL CS pin is disabled and the output has an internal pull-up to 3.3 V. The CTRL CS pin can be left open when not used. The logic options for the secondary remote control can be positive or negative logic.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. Minimum

recommended external input capacitance is 100 μ F. The performance in some applications can be enhanced by addition of external capacitance as described under External Decoupling Capacitors.

External Decoupling Capacitors

When powering loads with significant dynamic current requirements, the voltage regulation at the point of load can be improved by addition of decoupling capacitors at the load. The recommended minimum capacitance on the output is 100 μ F. The most effective technique is to locate low ESR ceramic and electrolytic capacitors as close to the load as possible, using several parallel capacitors to lower the effective ESR. The ceramic capacitors will handle high-frequency dynamic load changes while the electrolytic capacitors are used to handle low frequency dynamic load changes. Ceramic capacitors will also reduce any high frequency noise across the load. It is equally important to use low resistance and low inductance PWB layouts and cabling.

External decoupling capacitors will become part of the product's control loop. The control loop is optimized for a wide range of external capacitance and the maximum recommended value that could be used without any additional analysis is found in the Electrical specification.

The ESR of the capacitors is a very important parameter. Stable operation is guaranteed with a verified ESR value of >10 m Ω across the output connections.

For further information please contact your local Ericsson Power Modules representative.

PMBus configuration and support

The products provide a PMBus digital interface that enables the user to configure many aspects of the device operation as well as monitor the input and output parameters. Please contact your local Ericsson Power Modules representative for appropriate SW tools to down-load new configurations.

Output Voltage Adjust using PMBus

The output voltage of the product can be reconfigured using the PMBus interface. BMR 453 xx00/001 and /002 can be adjusted from 8.1 V to 13.2 V. The BMR 453 xx02/003 and /004 can be adjusted from 3.0 V to 6.7 V.

Margin Up/Down Controls

These controls allow the output voltage to be momentarily adjusted, either up or down, by a nominal 10%. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors.

The margin up and down levels of the product can be re-configured using the PMBus interface.

Soft-start Power Up

The soft-start control introduces a time-delay (default setting 40 ms) before allowing the output voltage to rise. The default rise time of the ramp up is 10 ms. Power-up is hence completed within 50 ms in default configuration using remote control. When starting by applying input voltage the control circuit boot-up time adds an additional 100 ms delay. The soft-

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start power up of the product can be reconfigured using the PMBus interface.

Remote Sense

The products have remote sense that can be used to compensate for voltage drops between the output and the point of load. The sense traces should be located close to the PCB ground layer to reduce noise susceptibility. The remote sense circuitry will compensate for up to 10% voltage drop between +Out pin and the point of load (+Sense). The -Sense pin should be always connected to -Out. When activating remote sense, connect the +Sense pin to the +Input of the load. If the remote sense is not needed +Sense pin should be connected to +Out of the BMR453 unit. To be able to use remote sense the converter must be equipped with a digital connector.

Temperature Protection (OTP, UTP)

The products are protected from thermal overload by an internal temperature shutdown protection. When T_{P1} as defined in thermal consideration section is exceeded the product will shut down. The product will make continuous attempts to start up (non-latching mode) and resume normal operation automatically when the temperature has dropped below the temperature threshold, the hysteresis is defined in general electrical specification. The OTP and hysteresis of the product can be re-configured using the PMBus interface. The product has also an under temperature protection. The OTP and UTP fault limit and fault response can be configured via the PMBus. Note: using the fault response "continue without interruption" may cause permanent damage of the product.

Over Voltage Protection (OVP)

The product has output over voltage protection that will shut down the converter in over voltage conditions (latching mode). The OVP fault level and fault response can be re-configured using the PMBus interface.

Over Current Protection (OCP)

The product includes current limiting circuitry for protection at continuous overload. The product will enter hic-up mode if the maximum output current is exceeded and the output voltage is below $0.3 \times V_{out}$. The load distribution should be designed for the maximum output short circuit current specified. If for some reason the output should be short circuited, minimum resistance should not be lower than 6 m Ω . The OCP level and fault response can be re-configured using the PMBus interface. The default configuration is set to hic-up mode for the OCP, except for BMR453xxxx/001 (latching OCP).

Input Over/Under voltage protection

The input of the product can be protected against high input voltage and low input voltage. The over- and under-voltage fault level and fault response can be configured via the PMBus interface.

Pre-bias Start-up

The product has a Pre-bias start up functionality and will not sink current during start up if a pre-bias source is present at the output terminals.

Power Good

The PG SYNC pin can be configured as an output (POWER GOOD). The power good signal (TTL level) indicates proper operation of the product and can also be used as an error flag indicator. The PG SYNC pin has POWER GOOD as default configuration with the output set as active low. The PG SYNC pin is configured via the PMBus interface.

Tracking and External reference

The PG SYNC pin can be configured as an input for voltage tracking or an external analogue reference. The PG SYNC pin is configured via the PMBus interface and has default setting Power Good. Send command MFR_MULTI_PIN_CONFIG (0xF9h) with data 0x10h, the module will work in standalone tracking mode; Connect the PG_SYNC pin to the external reference voltage (ground to -OUT), the output voltage will follow this reference voltage with a predefined scale. The max reference voltage is 2.5 V which connects to digital controller's ADC port. The reference voltage / V_{out} scale factor is stored in MFR_VOUT_ANALOG_SCALE (0xE8h) with default value 0.175(0xA2CDh), end user can change it by using PMBus command. End user can read the scaled value by command MFR_READ_VOUT_ANALOG_REF (0xE9h). Any changes of using PMBUS command should use command Store Default all (0x11h) to make the change permanent before power off.

Switching frequency adjust using PMBus

The switching frequency is set to 140 kHz as default but this can be reconfigured via the PMBus interface. The product is optimized at this frequency but can run at lower and higher frequency, (125 kHz – 150 kHz). However the output performance is not specified if the frequency is changed.

Input Transient

The BMR453 products have limited ability to react on sudden input voltage changes. As an example the 12 V module BMR453xxxx/001 can have an output voltage deviation of 5 V when a 20 V input step is applied (40 V to 60 V). This is tested with a slew rate of 0.1 V/us on the input voltage change and minimum output capacitance 100 μ F. Increasing the output capacitance will improve the result.

Parallel Operation with Droop

The BMR 453 0006(or BMR4530007) with /012 or /013 or /014 configuration file are variants that can be connected in parallel. The products have a pre-configured voltage droop: The stated output voltage set point is at no load, The output voltage will decrease when the load current is increased, the voltage will droop 0.6V while load reaches max load. This feature allows

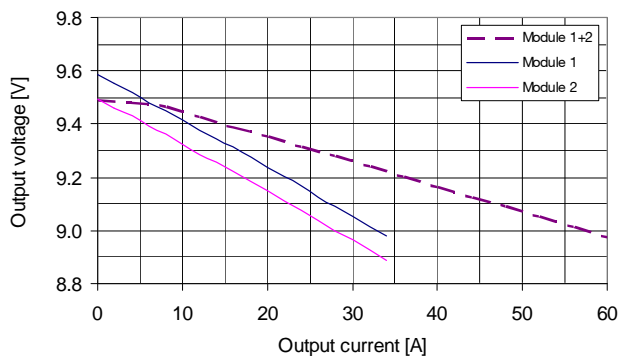
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the products to be connected in parallel and share the current with 10% accuracy. Up to 90% of max output current can be used from each module.

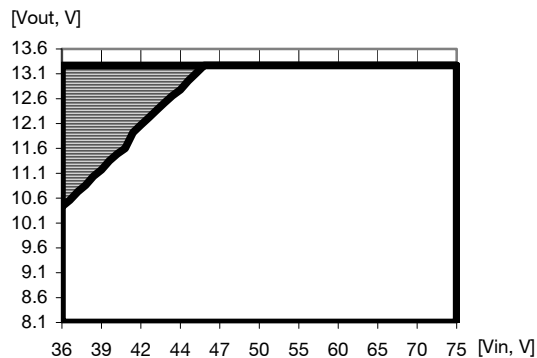
Parallel Operation with Droop


Fault protection at parallel operation with Droop

If one of the two modules exceeds the OVP, OCP or OTP level, the module might turn off depends on its pre-set fault response action, and the other module might not handle more current than its max capability, that will lead to both modules can not recover until the protection trig condition removed, to secure a normal operation, both modules need a reset.

Synchronization with Frequency Interleaving

In order to reduce the input line current ripple, two products may be synchronized including frequency interleaving. Similarly as in the parallel configuration one module must be configured as a master, the other one as a slave. Only the sync signal should be provided from the master to the slave module. The same switching frequency restrictions as for the paralleling are valid. When the PG SYNC pin is configured as an input (SYNC IN) the device will automatically check for a clock signal on the PG SYNC pin each time the module is enabled by RC or via PMBus.

BMR4530000/001 Output voltage regulation


Ordering operational designation n3 n4 = 00 or 01 , Output voltage set point vs input voltage at: TP1 = +25°C, IO = 33 A resistive load, The output voltage will be fully regulated for all operating combinations within the white area in the plot above. Operation outside of this area is not recommended for normal use. (Note 33 A is maximum load current at start-up)

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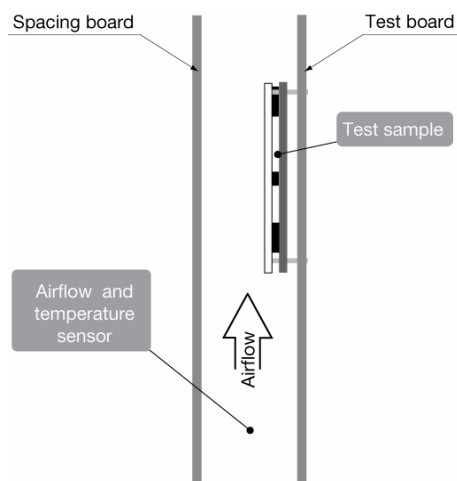
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Thermal Consideration

General

The products are designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation. For products mounted on a PWB without a heat sink attached, cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependant on the airflow across the product. Increased airflow enhances the cooling of the product. The Output Current Derating graph found in the Output section for each model provides the available output current vs. ambient air temperature and air velocity at $V_1 = 53$ V.

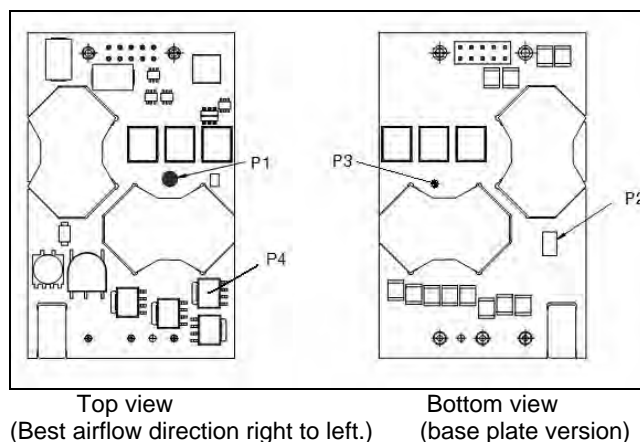
The product is tested on a 254 x 254 mm, 35 μ m (1 oz), 8-layer test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm.



Definition of product operating temperature

The product operating temperatures is used to monitor the temperature of the product, and proper thermal conditions can be verified by measuring the temperature at positions P1, P2, P3, P4. The temperature at these positions (T_{P1} , T_{P2} , T_{P3} , T_{P4}) should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above maximum T_{P1} , measured at the reference point P1 (P3 for base plate versions) are not allowed and may cause permanent damage.

Position	Description	Max temperature
P1	PWB (reference point)	$T_{P1} = 125^\circ \text{C}$
P2	Opto-coupler	$T_{P2} = 105^\circ \text{C}$
P3	PWB (reference point for base-plate version)	$T_{P3} = 125^\circ \text{C}$
P4	Primary MOSFET	$T_{P4} = 125^\circ \text{C}$



Ambient Temperature Calculation

For products with base plate the maximum allowed ambient temperature can be calculated by using the thermal resistance.

1. The power loss is calculated by using the formula $((1/\eta) - 1) \times \text{output power} = \text{power losses (Pd)}$. η = efficiency of product. E.g. 95% = 0.95
2. Find the thermal resistance (R_{th}) in the Thermal Resistance graph found in the Output section for each model. **Note that the thermal resistance can be significantly reduced if a heat sink is mounted on the top of the base plate.**

Calculate the temperature increase (ΔT).

$$\Delta T = R_{th} \times P_d$$

3. Max allowed ambient temperature is:

$$\text{Max } T_{P1} - \Delta T.$$

E.g. BMR 453 5100/001 at 2 m/s:

1. $((\frac{1}{0.944}) - 1) \times 396 \text{ W} = 23.5 \text{ W}$
2. $23.5 \text{ W} \times 3.1^\circ \text{C/W} = 73^\circ \text{C}$
3. $125^\circ \text{C} - 73^\circ \text{C} = \text{max ambient temperature is } 52^\circ \text{C}$

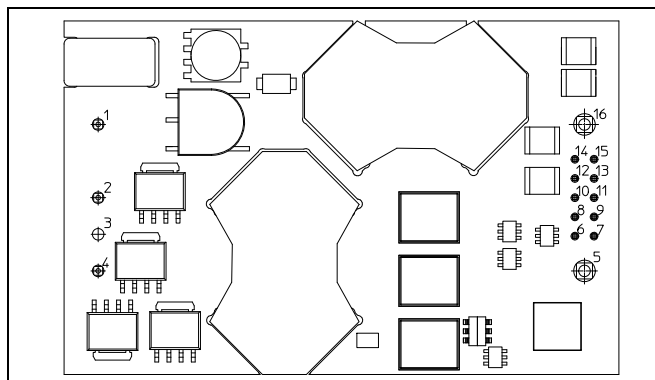
The actual temperature will be dependent on several factors such as the PWB size, number of layers and direction of airflow.

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 Input 36-75 V, Output up to 60 A / 396 W

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Connections (Top view)



Pin	Designation	Function
1	+In	Positive Input
2	RC	Remote Control
3	Case	Case to GND (optinal)
4	-In	Negative Input
5	-Out	Negative Output
6	S+	Positive Remote Sense
7	S-	Negative Remote Sense
8	SA0	Address pin 0
9	SA1	Address pin 1
10	SCL	PMBus Clock
11	SDA	PMBus Data
12	PG SYNC	Configurable I/O pin: Power Good output, SYNC-, tracking-, or ext ref-input
13	DGND	PMBus ground
14	SALERT	PMBus alert signal
15	CTRL CS	PMBus remote control or Current share
16	+Out	Positive Output

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PMBus Communications

The products provide a PMBus digital interface that enables the user to configure many aspects of the device operation as well as monitor the input and output parameters. The products can be used with any standard two-wire I²C or SMBus host device. In addition, the device is compatible with PMBus version 1.1 and includes an SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring.

Monitoring via PMBus

A system controller can monitor a wide variety of different parameters through the PMBus interface. The controller can monitor for fault condition by monitoring the SALERT pin, which will be asserted when any number of pre-configured fault or warning conditions occur. The system controller can also continuously monitor for any number of power conversion parameters including but not limited to the following:

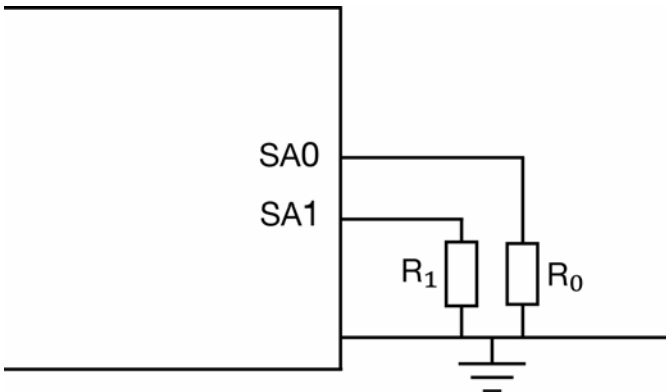
- Input voltage
- Output voltage
- Output current
- Internal junction temperature
- Switching frequency
- Duty cycle

Evaluation software

A Configuration Monitoring and Management (CMM) evaluation software, is available for the products. For more information please contact your local Ericsson Power Modules sales representative.

Addressing

The figure and table below show recommended resistor values with min and max voltage range for hard-wiring PMBus addresses (series E96, 1% tolerance resistors suggested):



SA0/SA1	R ₁ /R ₀ [kΩ]	Min voltage[V]	Max voltage[V]
0	24.9	0.261	0.438
1	49.9	0.524	0.679
2	75	0.749	0.871
3	100	0.926	1.024
4	124	1.065	1.146
5	150	1.187	1.256
6	174	1.285	1.345
7	200	1.371	1.428

The SA0 and SA1 pins can be configured with a resistor to GND according to the following equation.

PMBus Address = 8 x (SA0value) + (SA1 value)

If any one of those voltage applied to ADC0 and ADC1 is out of the range from the table above, PMBus address 127 is assigned. If the calculated PMBus address is 0 or 12, PMBus address 127 is assigned instead. PMBus address 11 is not to be used. The user shall also be aware of further limitations of the addresses as stated in the PMBus Specification.

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PMBus Commands

The DC/DC converter is PMBUS compliant. The following table lists the implemented PMBus commands. For more detailed information see PMBus Power System Management Protocol Specification; Part I – General Requirements, Transport and Electrical Interface and PMBus Power System Management Protocol; Part II – Command Language.

Designation	Cmd	Impl
Standard PMBus Commands		
Control Commands		
PAGE	00h	No
OPERATION	01h	Yes
ON_OFF_CONFIG	02h	Yes
WRITE_PROTECT	10h	Yes
Output Commands		
VOUT_MODE	20h	Yes
VOUT_COMMAND	21h	Yes
VOUT_TRIM	22h	Yes
VOUT_GAIN	23h	Yes ^{note1}
VOUT_MAX	24h	Yes
VOUT_MARGIN_HIGH	25h	Yes
VOUT_MARGIN_LOW	26h	Yes
VOUT_TRANSITION_RATE	27h	Yes
VOUT_DROOP	28h	No
VOUT_SCALE_LOOP	29h	Yes ^{note1}
VOUT_SCALE_MONITOR	2Ah	Yes ^{note1}
COEFFICIENTS	30h	No
POUT_MAX	31h	No
MAX_DUTY	32h	Yes
FREQUENCY_SWITCH	33h	Yes
VIN_ON	35h	Yes
VIN_OFF	36h	Yes
IOUT_CAL_GAIN	38h	Yes ^{note1}
IOUT_CAL_OFFSET	39h	Yes ^{note1}
Fault Limit Commands		
POWER_GOOD_ON	5Eh	Yes
POWER_GOOD_OFF	5Fh	Yes
VOUT_OV_FAULT_LIMIT	40h	Yes
VOUT_UV_FAULT_LIMIT	44h	Yes
IOUT_OC_FAULT_LIMIT	46h	Yes
IOUT_OC_LV_FAULT_LIMIT	48h	Yes
IOUT_UC_FAULT_LIMIT	4Bh	No
OT_FAULT_LIMIT	4Fh	Yes

Designation	Cmd	Impl
OT_WARN_LIMIT	51h	Yes
UT_WARN_LIMIT	52h	Yes
UT_FAULT_LIMIT	53h	Yes
VIN_OV_FAULT_LIMIT	55h	Yes
VIN_OV_WARN_LIMIT	57h	Yes
VIN_UV_WARN_LIMIT	58h	Yes
VIN_UV_FAULT_LIMIT	59h	Yes
VOUT_OV_WARN_LIMIT	42h	Yes
VOUT_UV_WARN_LIMIT	43h	Yes
IOUT_OC_WARN_LIMIT	4Ah	Yes
IIN_OC_FAULT_LIMIT	5Bh	No
IIN_OC_WARN_LIMIT	5Dh	No
Fault Response Commands		
VOUT_OV_FAULT_RESPONSE	41h	Yes
VOUT_UV_FAULT_RESPONSE	45h	Yes
OT_FAULT_RESPONSE	50h	Yes
UT_FAULT_RESPONSE	54h	Yes
VIN_OV_FAULT_RESPONSE	56h	Yes
VIN_UV_FAULT_RESPONSE	5Ah	Yes
IOUT_OC_FAULT_RESPONSE	47h	Yes
IOUT_UC_FAULT_RESPONSE	4Ch	No
IIN_OC_FAULT_RESPONSE	5Ch	No
Time setting Commands		
TON_DELAY	60h	Yes
TON_RISE	61h	Yes
TON_MAX_FAULT_LIMIT	62h	Yes
TON_MAX_FAULT_RESPONSE	63h	Yes
TOFF_DELAY	64h	Yes
TOFF_FALL	65h	Yes
TOFF_MAX_WARN_LIMIT	66h	Yes
Status Commands (Read Only)		
CLEAR_FAULTS	03h	Yes
STATUS_BYTES	78h	Yes
STATUS_WORD	79h	Yes
STATUS_VOUT	7Ah	Yes
STATUS_IOUT	7Bh	Yes
STATUS_INPUT	7Ch	Yes
STATUS_TEMPERATURE	7Dh	Yes
STATUS_CML	7Eh	Yes
STATUS_OTHER	7Fh	Yes
Monitor Commands (Read Only)		
READ_VIN	88h	Yes

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Designation	Cmd	Impl
READ_VOUT	8Bh	Yes
READ_IOUT	8Ch	Yes
READ_TEMPERATURE_1	8Dh	Yes
READ_TEMPERATURE_2	8Eh	Yes
READ_FAN_SPEED_1	90h	No
READ_DUTY_CYCLE	94h	Yes
READ_FREQUENCY	95h	Yes
READ_POUT	96h	No
READ_PIN	97h	No
Identification Commands (Read Only)		
PMBUS_REVISION	98h	Yes
MFR_ID	99h	Yes ^{note1}
MFR_MODEL	9Ah	Yes ^{note1}
MFR_REVISION	9Bh	Yes ^{note1}
MFR_LOCATION	9Ch	Yes ^{note1}
MFR_DATE	9Dh	Yes ^{note1}
MFR_SERIAL	9Eh	Yes ^{note1}
Group Commands		
INTERLEAVE	37h	No
Supervisory Commands		
STORE_DEFAULT_ALL	11h	Yes
RESTORE_DEFAULT_ALL	12h	Yes
STORE_USER_ALL	15h	No
RESTORE_USER_ALL	16h	No
BMR 453/454 Specific Commands		
MFR_POWER_GOOD_POLARITY	D0h	Yes
MFR_VOUT_UPPER_RESISTOR	D2h	Yes ^{note1}
MFR_VIN_SCALE_MONITOR	D3h	Yes ^{note1}
MFR_CLA_TABLE_NUM_ROW	D4h	Yes
MFR_CLA_ROW_COEFFICIENTS	D5h	Yes
MFR_STORE_CLA_TABLE	D6h	Yes
MFR_ACTIVE_COEFF_CLA_TABLE	D8h	Yes
MFR_SET_ROM_MODE	D9h	Yes ^{note1}
MFR_SELECT_TEMP_SENSOR	DCh	Yes
MFR_VIN_OFFSET	DDh	Yes ^{note1}
MFR_REMOTE_TEMP_CAL	E2h	Yes
MFR_REMOTE_CONTROL	E3h	Yes
MFR_DEAD_BAND_MODE	E4h	Yes ^{note1}
MFR_DEAD_BAND_DELAY	E5h	Yes ^{note1}
MFR_TEMP_COEFF	E7h	Yes ^{note1}
MFR_VOUT_ANALOG_SCALE	E8h	Yes
MFR_READ_VOUT_ANALOG_REF	E9h	Yes

Designation	Cmd	Impl
MFR_DEBUG_BUFF	F0h	Yes
MFR_SETUP_PASSWORD	F1h	Yes
MFR_DISABLE_SECURITY	F2h	Yes
MFR_DEAD_BAND_IOUT_THRESHOLD	F3h	Yes ^{note1}
MFR_SECURITY_BIT_MASK	F4h	Yes
MFR_PRIMARY_TURN	F5h	Yes ^{note1}
MFR_SECONDARY_TURN	F6h	Yes ^{note1}
MFR_SET_DPWM_POLARITY	F7h	Yes ^{note1}
MFR_ILIM_SOFTSTART	F8h	Yes
MFR_MULTI_PIN_CONFIG	F9h	Yes
MFR_DEAD_BAND_VIN_THRESHOLD	FAh	Yes ^{note1}
MFR_DEAD_BAND_VIN_IOUT_HYS	FBh	Yes ^{note1}
MFR_FIRMWARE_VERSION	FCh	Yes ^{note1}
MFR_MESSAGE_CODE_DEVICE_ID	FDh	Yes ^{note1}

Notes:

Cmd is short for Command.

Impl is short for Implemented.

Note1:

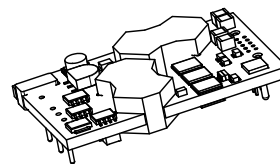
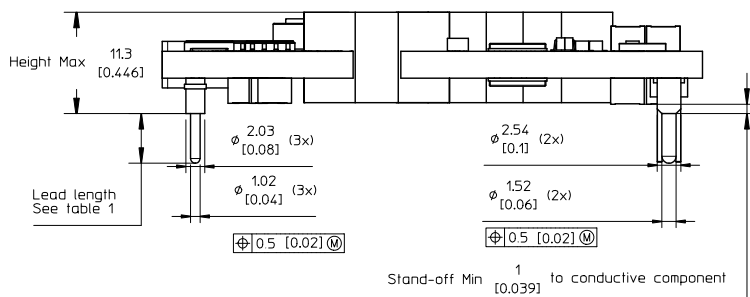
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BMR 453 series Fully regulated Intermediate Bus Converters
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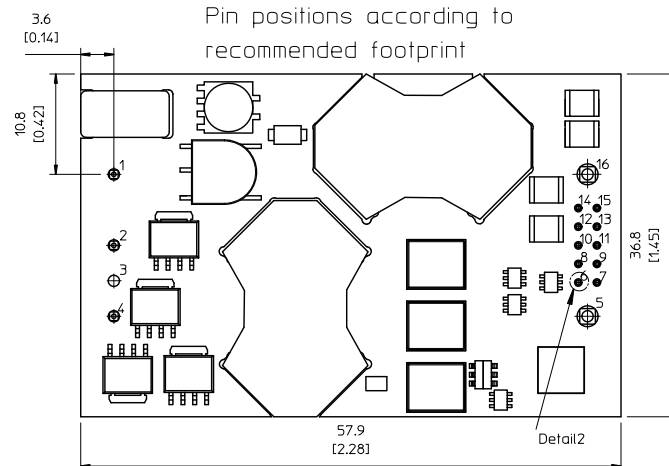
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Mechanical Information - Hole Mount, Open Frame Version

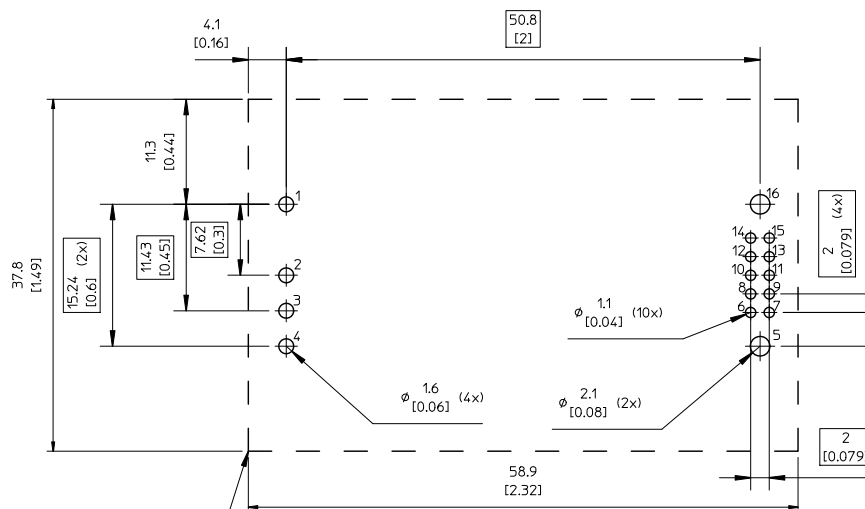


TOP VIEW

Pin positions according to
recommended footprint

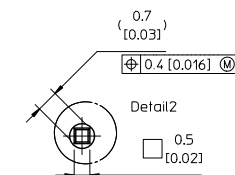


RECOMMENDED FOOTPRINT - TOP VIEW



Recommended keep away area for user components.

The stand-off in combination with insulating material ensures that requirements as per IEC/EN/UL60950 are met and 1500 V isolation maintained even if open vias or traces are present under the DC/DC converter.



Digital connector pins (10x)

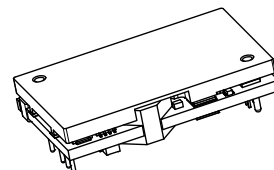
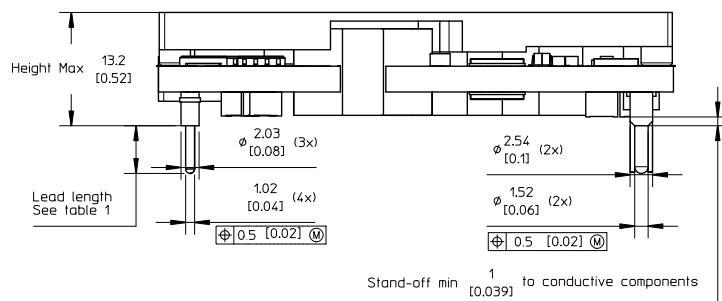
Weight: Typical 48 g
All dimensions in mm [inch].
Tolerances unless specified:
x.x ±0.50 [0.02], x.xx±0.25 [0.01]
(not applied on footprint or typical values)



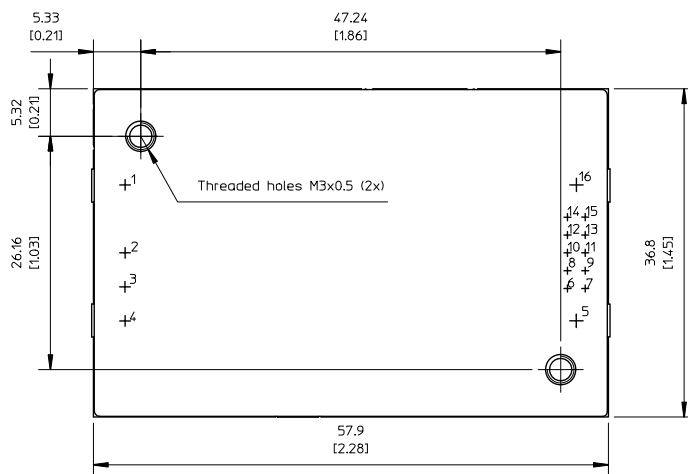
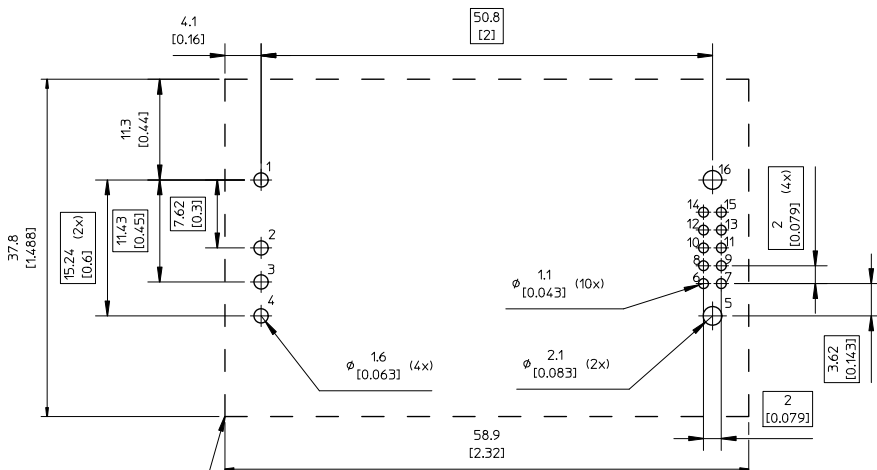
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Mechanical Information- Hole Mount, Base Plate Version

TOP VIEW

Pin positions according to recommended footprint


RECOMMENDED FOOTPRINT - TOP VIEW


Recommended keep away area for user components.

The stand-off in combination with insulating material ensures that requirements as per IEC/EN/UL60950 are met and 1500 V isolation maintained even if open vias or traces are present under the DC/DC converter.

X1	Lead length
0	5.33 [0.210]
2	3.69 [0.145] (cut)
3	4.57 [0.180] (cut)
4	2.79 [0.110] (cut)
5	2.79 [0.110]

Table 1.

X1 = Ordering information

CASE

Material: Aluminium

For screw attachment apply mounting torque of max 0.44 Nm [3.9 lbf in]. M3 screws must not protrude more than 2.7 mm [0.106] in to the base plate.

PIN SPECIFICATIONS

Pin 1,2,3,4,5 & 16 Material: Copper Alloy

Plating: Min Au 0.1µm over 1-3µm Ni.

Pin 6-15 Material: Brass

Plating: Min Au 0.2µm over 1.3µm Ni.

NOTE

Pin 6-15 are optional and only used if digital communication is requested.

Pin 3 is only used for baseplate GND connection.

X1-5 Are special customer pins with extra stand off 6.7 mm & Max height 18.9 mm.

Weight: Typical 67 g

All dimensions in mm [inch].

Tolerances unless specified:

x.x +0.50 [0.02], x.xx+0.25 [0.01]

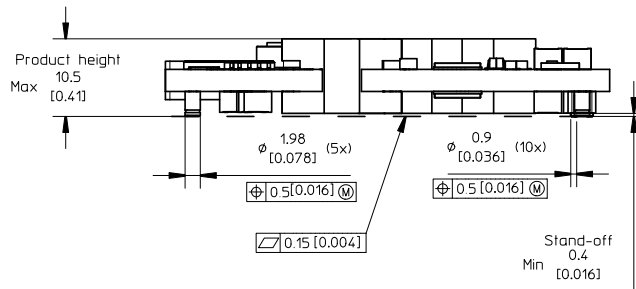
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BMR 453 series Fully regulated Intermediate Bus Converters
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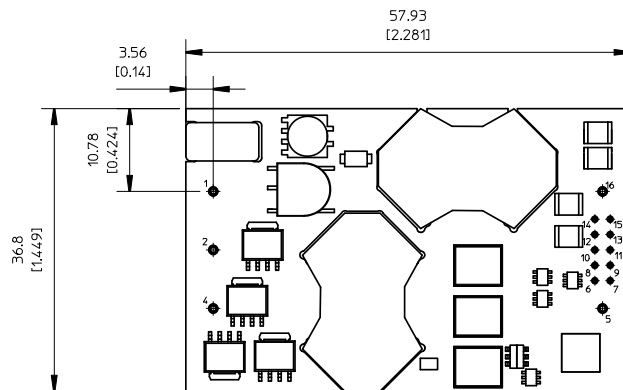
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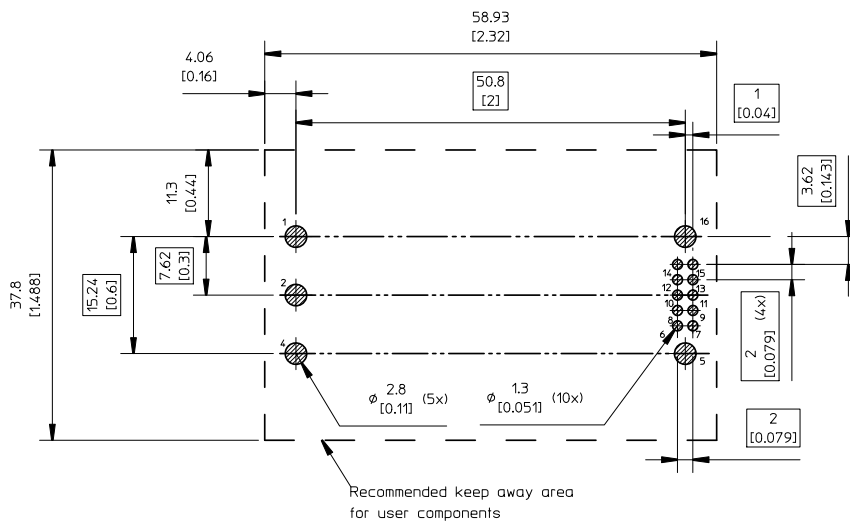
Mechanical Information - SMD mount, Open Frame Version


TOP VIEW

Pin positions according to recommended footprint



RECOMMENDED FOOTPRINT - TOP VIEW


NOTES
PIN SPECIFICATIONS

Pin 1,2,4,5 & 16 - Material: Copper alloy

 Plating: Au 0.1 μ m over 1-3 μ m Ni.

Pin 6-15 - Material: Brass

 Plating: Au 0.1 μ m over 2 μ m Ni.

Weight: Typical 46 g

All dimensions in mm [inch].

Tolerances unless specified:

 x.x \pm 0.5 mm [0.02]

 x.xx \pm 0.25 mm [0.01]

(not applied on footprint or typical values)

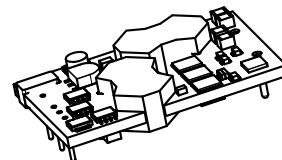
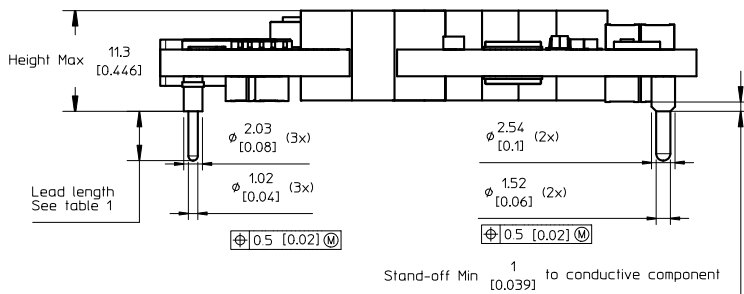


BMR 453 series Fully regulated Intermediate Bus Converters
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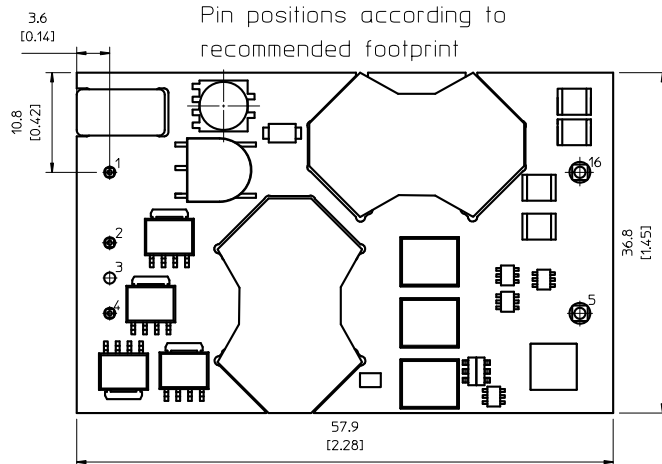
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Mechanical Information - Hole mount, Open Frame Version, Non Digital Interface



TOP VIEW

Pin positions according to recommended footprint



X1	Lead length
0	5.33 [0.210]
2	3.69 [0.145] (cut)
3	4.57 [0.180] (cut)
4	2.79 [0.110] (cut)
5	2.79 [0.110]

Table 1.

X1 = Ordering information

PIN SPECIFICATIONS

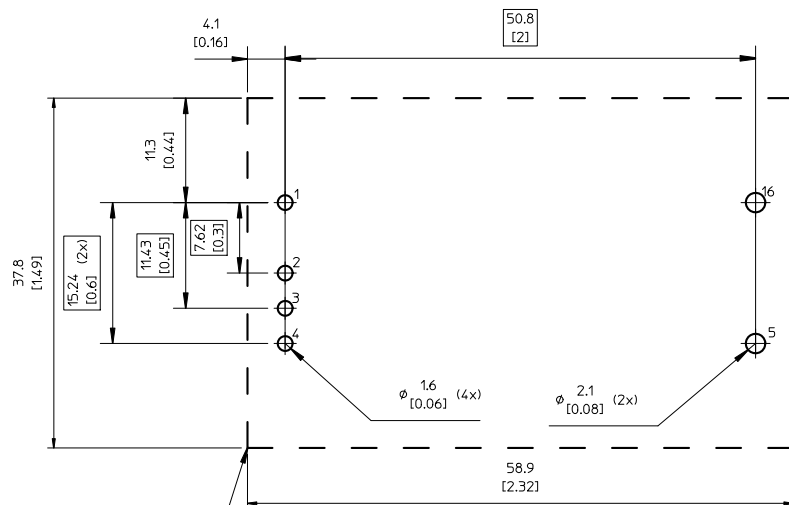
Pin 1,2,4,5 & 16 Material: Copper alloy
Plating: Min Au 0.1 μ m over 1-3 μ m Ni.

NOTE:

X1-5 Are special customer pins with extra stand off 6.7 mm & Max Height 17 mm.

Position 3 is only used for base plate GND connection pin.

RECOMMENDED FOOTPRINT - TOP VIEW



Recommended keep away area for user components.

The stand-off in combination with insulating material ensures that requirements as per IEC/EN/UL60950 are met and 1500 V isolation maintained even if open vias or traces are present under the DC/DC converter.

Weight: Typical 48 g

All dimensions in mm [inch].

Tolerances unless specified:

x.x \pm 0.50 [0.02], x.xx \pm 0.25 [0.01]

(not applied on footprint or typical values)



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Soldering Information – Surface Mounting

The surface mount product is intended for forced convection or vapor phase reflow soldering in SnPb and Pb-free processes.

The reflow profile should be optimised to avoid excessive heating of the product. It is recommended to have a sufficiently extended preheat time to ensure an even temperature across the host PCB and it is also recommended to minimize the time in reflow.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long time reliability and isolation voltage.

Minimum Pin Temperature Recommendations

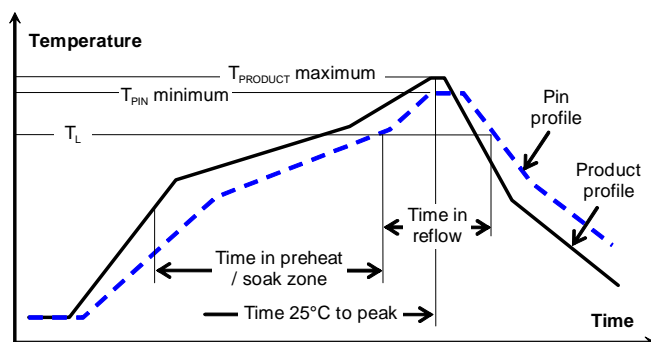
Pin number 5 is chosen as reference location for the minimum pin temperature recommendation since this will likely be the coolest solder joint during the reflow process.

SnPb solder processes

For SnPb solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature, (T_L , 183°C for Sn63Pb37) for more than 30 seconds and a peak temperature of 210°C is recommended to ensure a reliable solder joint.

For dry packed products only: depending on the type of solder paste and flux system used on the host board, up to a recommended maximum temperature of 245°C could be used, if the products are kept in a controlled environment (dry pack handling and storage) prior to assembly.

General reflow process specifications		SnPb eutectic	Pb-free
Average ramp-up ($T_{PRODUCT}$)		3°C/s max	3°C/s max
Typical solder melting (liquidus) temperature	T_L	183°C	221°C
Minimum reflow time above T_L		30 s	30 s
Minimum pin temperature	T_{PIN}	210°C	235°C
Peak product temperature	$T_{PRODUCT}$	225°C	260°C
Average ramp-down ($T_{PRODUCT}$)		6°C/s max	6°C/s max
Maximum time 25°C to peak		6 minutes	8 minutes


Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature (T_L , 217 to 221°C for SnAgCu solder alloys) for more than 30 seconds and a peak temperature of 235°C on all solder joints is recommended to ensure a reliable solder joint.

Maximum Product Temperature Requirements

Top of the product PCB near pin 2 is chosen as reference location for the maximum (peak) allowed product temperature ($T_{PRODUCT}$) since this will likely be the warmest part of the product during the reflow process.

SnPb solder processes

For SnPb solder processes, the product is qualified for MSL 1 according to IPC/JEDEC standard J-STD-020C.

During reflow $T_{PRODUCT}$ must not exceed 225 °C at any time.

Pb-free solder processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C.

During reflow $T_{PRODUCT}$ must not exceed 260 °C at any time.

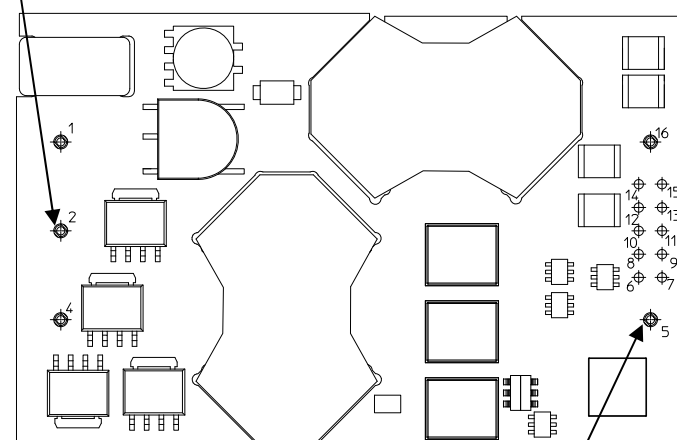
Dry Pack Information

Products intended for Pb-free reflow soldering processes are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033 (Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices).

Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J-STD-033.

Thermocoupler Attachment

Pin 2 for measurement of maximum product temperature $T_{PRODUCT}$



Pin 5 for measurement of minimum Pin (solder joint) temperature T_{PIN}

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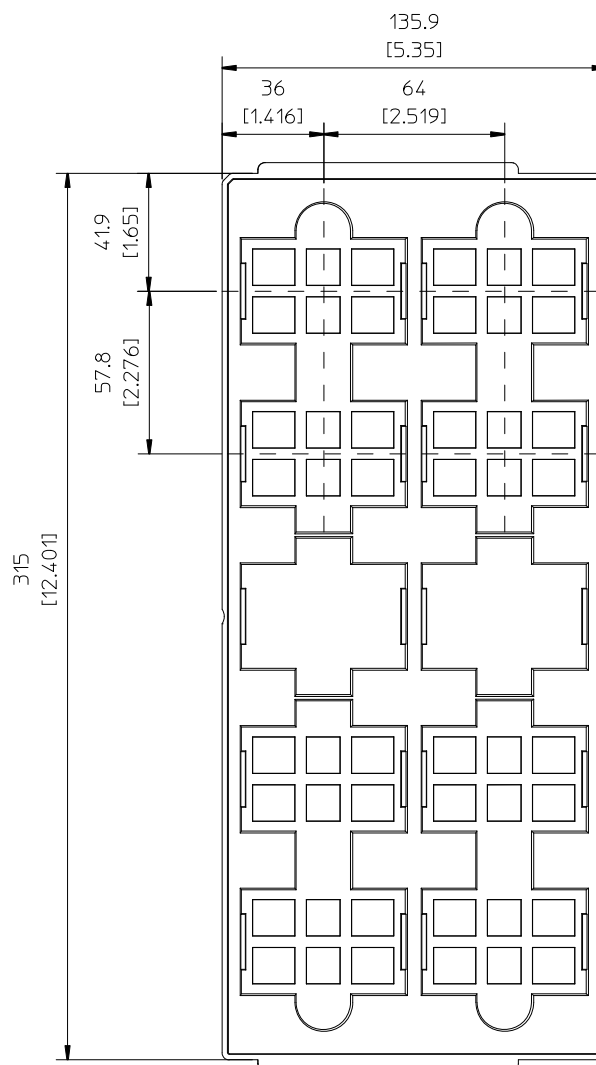
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Delivery Package Information – Surface Mount Version

The products are delivered in antistatic injection molded trays (Jedec design guide 4.10D standard).

Tray Specifications	
Material	Antistatic PPE
Surface resistance	$10^5 < \text{Ohm/square} < 10^{12}$
Bakability	The trays can be baked at maximum 125°C for 48 hours
Tray thickness	14.50 mm 0.571 [inch]
Box capacity	20 products (2 full trays/box)
Tray weight	125 g empty, 574 g full tray



JEDEC standard tray for 2x5 = 10 products.

All dimensions in mm [inch]

Tolerances: X.x ± 0.26 [0.01], X.xx ± 0.13 [0.005]

Note: pick up positions refer to center of pocket.
See mechanical drawing for exact location on product.

BMR 453 series Fully regulated Intermediate Bus Converters
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Soldering Information – Hole Mounting

The hole mounted product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds.

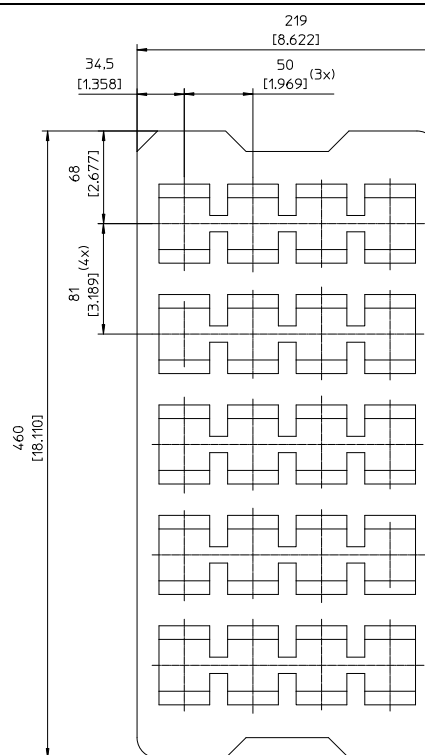
A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

Delivery Package Information – Hole Mount Version

The products are delivered in antistatic trays.

Tray Specifications	
Material	PE Foam
Surface resistance	$10^5 < \text{Ohm/square} < 10^{12}$
Bakability	The trays are not bakeable
Tray capacity	20 converters/tray
Box capacity	40 products (2 full trays/box)
Weight	Product – Open frame 1100 g full tray, 140g empty tray Product – Base plate option 1480 g full tray, 140 g empty tray



BMR 453 series Fully regulated Intermediate Bus Converters Input 36-75 V, Output up to 60 A / 396 W	EN/LZT 146 395 R6A July 2011
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Product Qualification Specification

Characteristics	
External visual inspection	IPC-A-610
Change of temperature (Temperature cycling)	IEC 60068-2-14 Na Temperature range Number of cycles Dwell/transfer time
Cold (in operation)	IEC 60068-2-1 Ad Temperature T _A Duration
Damp heat	IEC 60068-2-67 Cy Temperature Humidity Duration
Dry heat	IEC 60068-2-2 Bd Temperature Duration
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115 Human body model (HBM) Machine Model (MM)
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2 Water Glycol ether Isopropyl alcohol
Mechanical shock	IEC 60068-2-27 Ea Peak acceleration Duration
Moisture reflow sensitivity ¹	J-STD-020C Level 1 (SnPb-eutectic) Level 3 (Pb Free)
Operational life test	MIL-STD-202G, method 108A Duration
Resistance to soldering heat ²	IEC 60068-2-20 Tb, method 1A Solder temperature Duration
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1 Through hole mount products Surface mount products
Solderability	IEC 60068-2-58 test Td ¹ Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free
	IEC 60068-2-20 test Ta ² Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free
Vibration, broad band random	IEC 60068-2-64 Fh, method 1 Frequency Spectral density Duration

Notes
¹ Only for products intended for reflow soldering (surface mount products)

² Only for products intended for wave soldering (plated through hole products)

BMR 453 PI series Intermediate Bus Converters Input 44-75 V, Output up to 60 A / 711 W	EN/LZT 146 444 R1B August 2011
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Key Features

- Industry standard Quarter-brick footprint
57.9 x 36.8 x 24.5 mm (2.28 x 1.45 x 0.965 in)
- High efficiency, typ. 96.7% at 12.45 Vout half load
- 1500 Vdc input to output isolation
- Meets safety requirements according to IEC/EN/UL 60950-1
- MTBF 1.2 Mh

General Characteristics

- Output over voltage protection
- Input under voltage shutdown
- Over temperature protection
- Over current protection
- Remote control
- Highly automated manufacturing ensures quality
- ISO 9001/14001 certified supplier



Safety Approvals



Design for Environment



Meets requirements in high-temperature lead-free soldering processes.

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BMR 453 PI series Intermediate Bus Converters
 Input 44-75 V, Output up to 60 A / 711 W

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Ordering Information

Product program	Output
BMR4530108/014	12.45 V / 60 A, 711 W

Product Number and Packaging

BMR453	n ₁	n ₂	n ₃	n ₄	/	n ₅	n ₆	n ₇
Mechanical pin option	x				/			
Mechanical option		x			/			
Hardware option			x	x	/			
Configuration file					/	x	x	x

Optional designation	Description
n ₁	0 = Standard pin length 5.33 mm
n ₂	1 = Baseplate 2 = Baseplate with GND-pin
n ₃ n ₄	08 = 8.1-13.2 Vout Without digital interface
n ₅ n ₆ n ₇	014 = 12.45 V with 0.6 V droop load sharing function configuration
Packaging	20 converters/tray/box PE foam dissipative

Example: Product number BMR4530108/14 equals a Through hole mount lead length 5.33 mm, baseplate, without digital interface with 12.45 V standard configuration variant.
 For application specific configurations contact your local Ericsson Power Modules sales representative.

General Information
Reliability

The failure rate (λ) and mean time between failures (MTBF = $1/\lambda$) is calculated at max output power and an operating ambient temperature (T_A) of +40°C. Ericsson Power Modules uses Telcordia SR-332 Issue 2 Method 1 to calculate the mean steady-state failure rate and standard deviation (σ).

Telcordia SR-332 Issue 2 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

Mean steady-state failure rate, λ	Std. deviation, σ
804 nFailures/h	61 nFailures/h

MTBF (mean value) for the BMR453 series = 1.2 Mh.
 MTBF at 90% confidence level = 1.0 Mh

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2002/95/EC and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Ericsson Power Modules products are found in the Statement of Compliance document.

Ericsson Power Modules fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals (REACH) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of the products.

Warranty

Warranty period and conditions are defined in Ericsson Power Modules General Terms and Conditions of Sale.

Limitation of Liability

Ericsson Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

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Safety Specification

General information

Ericsson Power Modules DC/DC converters and DC/DC regulators are designed in accordance with safety standards IEC/EN/UL 60950-1 *Safety of Information Technology Equipment*.

IEC/EN/UL 60950-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Energy hazards
- Fire
- Mechanical and heat hazards
- Radiation hazards
- Chemical hazards

On-board DC/DC converters and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without "Conditions of Acceptability". Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use should comply with the requirements in IEC 60950-1, EN 60950-1 and UL 60950-1 *Safety of Information Technology Equipment*. There are other more product related standards, e.g. IEEE 802.3 CSMA/CD (Ethernet) Access Method, and ETS-300132-2 *Power supply interface at the input to telecommunications equipment, operated by direct current (dc)*, but all of these standards are based on IEC/EN/UL 60950-1 with regards to safety. Ericsson Power Modules DC/DC converters and DC/DC regulators are UL 60950-1 recognized and certified in accordance with EN 60950-1.

The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

The products should be installed in the end-use equipment, in accordance with the requirements of the ultimate application. Normally the output of the DC/DC converter is considered as SELV (Safety Extra Low Voltage) and the input source must be isolated by minimum Double or Reinforced Insulation from the primary circuit (AC mains) in accordance with IEC/EN/UL 60950-1.

Isolated DC/DC converters

It is recommended that a slow blow fuse is to be used at the input of each DC/DC converter. If an input filter is used in the circuit the fuse should be placed in front of the input filter.

In the rare event of a component problem that imposes a short circuit on the input source, this fuse will provide the following functions:

- Isolate the fault from the input power source so as not to affect the operation of other parts of the system.
- Protect the distribution wiring from excessive current and power loss thus preventing hazardous overheating.

The galvanic isolation is verified in an electric strength test. The test voltage (V_{iso}) between input and output is 1500 Vdc or 2250 Vdc (refer to product specification).

24 V DC systems

The input voltage to the DC/DC converter is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

48 and 60 V DC systems

If the input voltage to the DC/DC converter is 75 Vdc or less, then the output remains SELV (Safety Extra Low Voltage) under normal and abnormal operating conditions.

Single fault testing in the input power supply circuit should be performed with the DC/DC converter connected to demonstrate that the input voltage does not exceed 75 Vdc.

If the input power source circuit is a DC power system, the source may be treated as a TNV-2 circuit and testing has demonstrated compliance with SELV limits in accordance with IEC/EN/UL60950-1.

Non-isolated DC/DC regulators

The input voltage to the DC/DC regulator is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

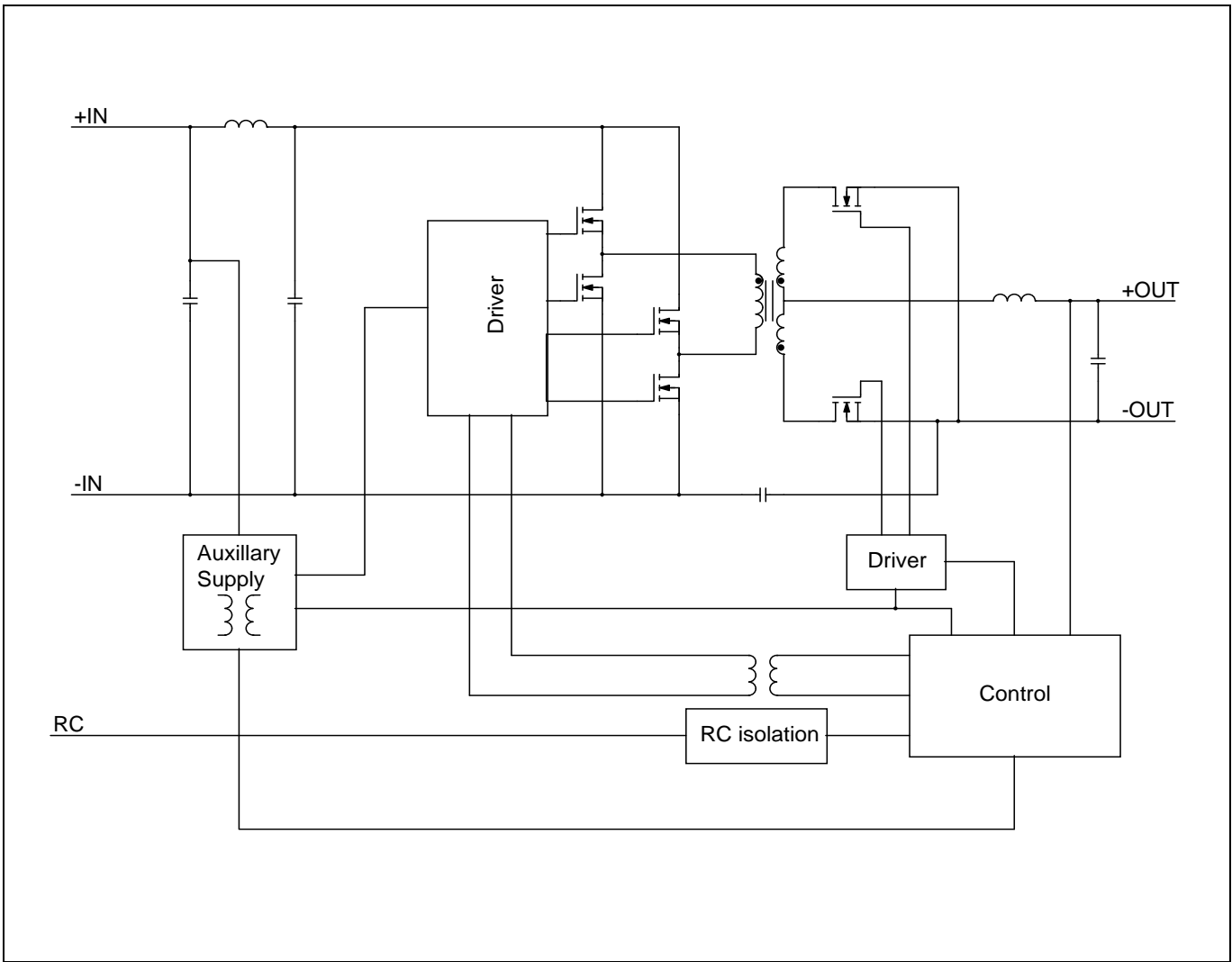
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Absolute Maximum Ratings

Characteristics			min	typ	max	Unit
T _{P1}	Operating Temperature (see Thermal Consideration section)		-40		+125	°C
T _S	Storage temperature		-55		+125	°C
V _I	Input voltage		-0.5		+80	V
V _{iso}	Isolation voltage (input to output test voltage)				1500	Vdc
V _{tr}	Input voltage transient (Tp 100ms)				100	V
V _{RC}	Remote Control pin voltage (see Operating Information section)	Positive logic option	-0.3		18	V
		Negative logic option	-0.3		18	V
V	SALERT, CTRL, SYNC, SCL, SDA, SA(0,1)		-0.3		3.6	V

Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits in the Electrical Specification. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.

Fundamental Circuit Diagram



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Electrical Specification
12.45 V, 60 A / 711 W
BMR 453 0208/014
 $T_{P1} = -40$ to $+90^{\circ}\text{C}$, $V_I = 44$ to 75 V, unless otherwise specified under Conditions.

 Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, max I_O , unless otherwise specified under Conditions.

 Additional $C_{in} = C_{out} = 220$ μF . See Operating Information section for selection of capacitor types.

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage range		44		75	V
V_{loff}	Turn-off input voltage	Decreasing input voltage	32.9	34.1	35.0	V
V_{lon}	Turn-on input voltage	Increasing input voltage	33.8	34.6	36.1	V
C_I	Internal input capacitance			35.2		μF
P_O	Output power		0		711	W
η	Efficiency	50% of max I_O		96.7		%
		max I_O		95.8		
		50% of max I_O , $V_I = 44$ V		96.9		
		max I_O , $V_I = 44$ V		95.8		
P_d	Power Dissipation	max I_O		31.2		W
P_{li}	Input idling power	$I_O = 0$ A, $V_I = 53$ V		4.8		W
P_{RC}	Input standby power	$V_I = 53$ V (turned off with RC)		0.32		W
f_s	Switching frequency	0-100 % of max I_O	133	140	145	kHz

V_{Oi}	Output voltage initial setting and accuracy	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, $I_O = 60$ A	12.40	12.42	12.43	V
V_O	Output voltage tolerance band	0-100% of max I_O	11.70		12.46	V
	Idling voltage	$I_O = 0$ A	12.4		12.4	V
	Line regulation	max I_O		20.0	21.0	mV
	Load regulation	$V_I = 53$ V, 1-100% of max I_O		510.2	661.0	mV
V_{tr}	Load transient voltage deviation	$V_I = 53$ V, Load step 25-75-25% of max I_O , $di/dt = 1$ A/ μs		± 320	± 400	mV
t_{tr}	Load transient recovery time	see Note 1		30		μs
t_r	Ramp-up time (from 10–90% of V_{Oi})	10-100% of max I_O	8.3	20.7	30.9	ms
t_s	Start-up time (from V_I connection to 90% of V_{Oi})		140.0	143.2	146.0	ms
t_f	V_I shut-down fall time (from V_I off to 10% of V_O)	max I_O		0.8		ms
t_{RC}	RC start-up time	max I_O		55.3		ms
	RC shut-down fall time (from RC off to 10% of V_O)	max I_O		3.3		ms
		$I_O = 0$ A		7.3		s
I_O	Output current		0		60	A
I_{lim}	Current limit threshold	$V_O = 10.8$ V	72.1	75	75	A
I_{sc}	Short circuit current	$T_{P1} = 25^{\circ}\text{C}$, see Note 2		77.5	84.9	A
C_{out}	Recommended Capacitive Load	$T_{P1} = 25^{\circ}\text{C}$	0.2	6.6	12	μF
V_{Oac}	Output ripple & noise, see Note3	See ripple & noise section, V_{Oi}		73.1	147.5	mVp-p
OVP	Over voltage protection	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, $I_O = 1$ A		15.8		V
RC	Sink current, see Note 4	See operating information			1.4	mA
	Trigger level	See operating information			1	V

 Note 1: $C_O = 6600$ μF OS-CON, 100 μF ceramic capacitor

Note 2: Applying load until the output voltage lower than 0.5V

Note 3: Low ESR-value

Note 4: Sink current drawn by external device connected to the RC pin. Minimum sink current required to guarantee activated RC function.

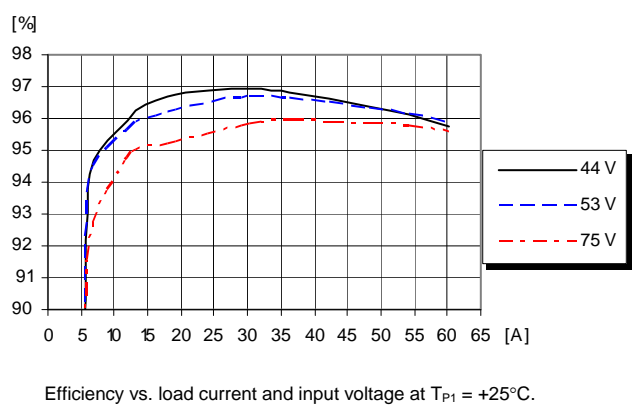
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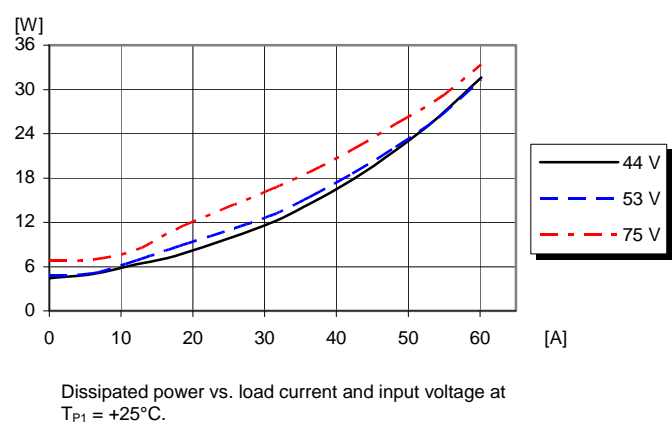
Typical Characteristics
12.45 V, 60 A / 711 W

BMR 453 0208/014

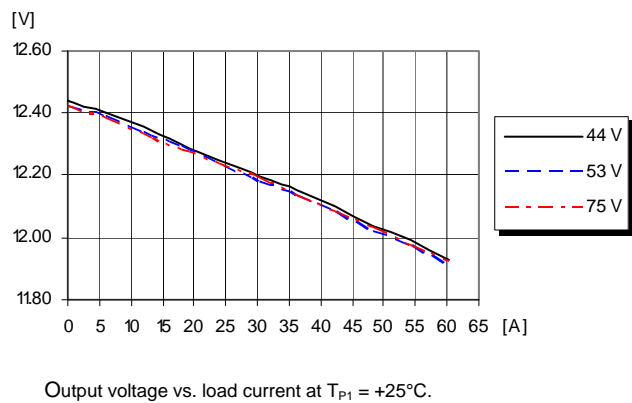
Efficiency



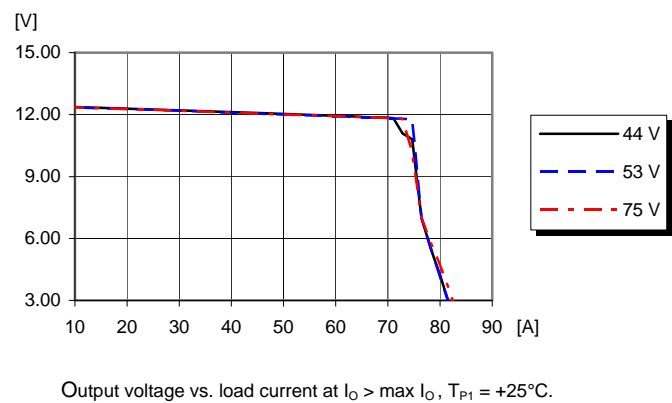
Power Dissipation



Output Characteristics



Current Limit Characteristics



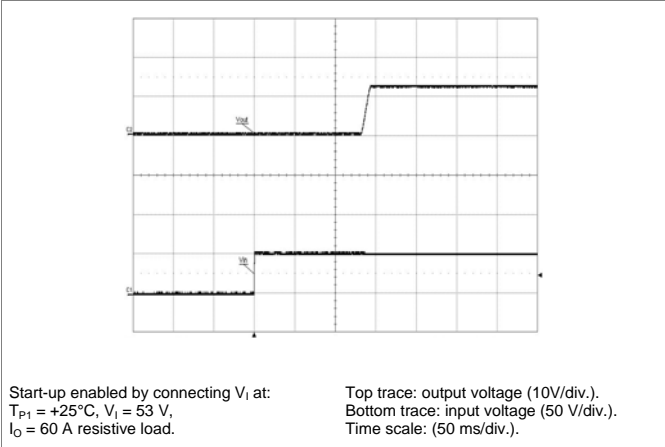
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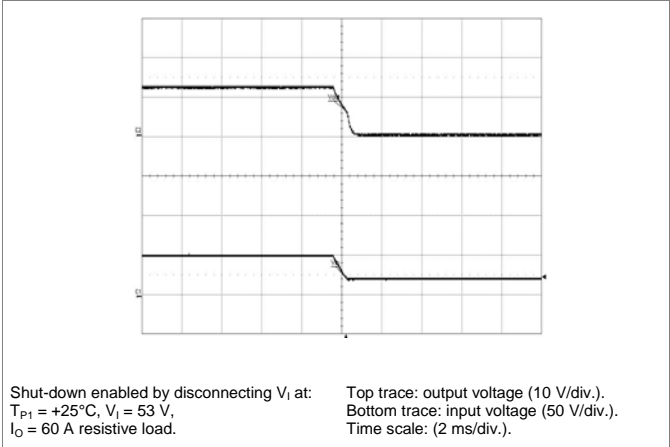
Typical Characteristics
12.45 V, 60 A / 711 W

BMR 453 0208/014

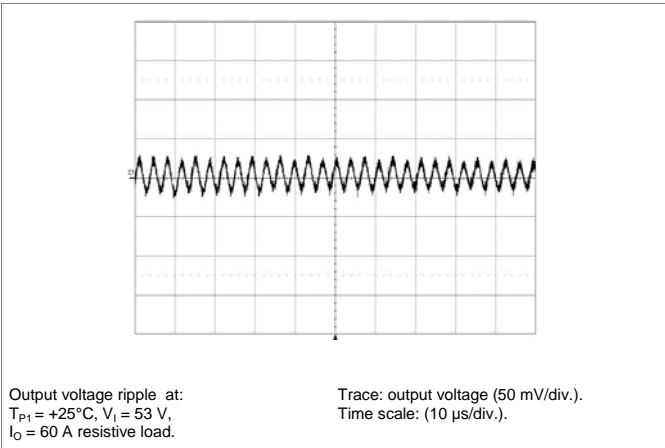
Start-up



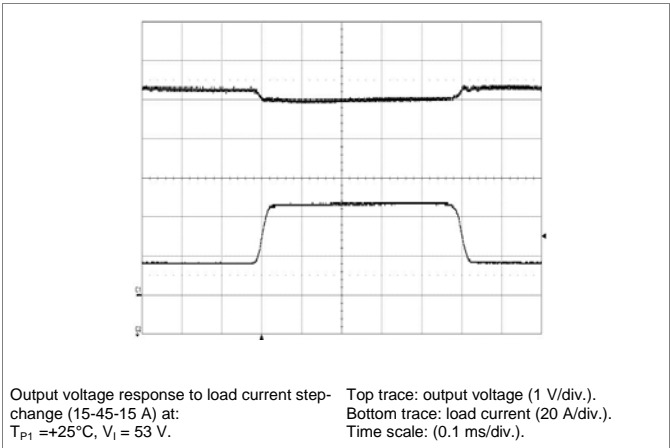
Shut-down



Output Ripple & Noise



Output Load Transient Response



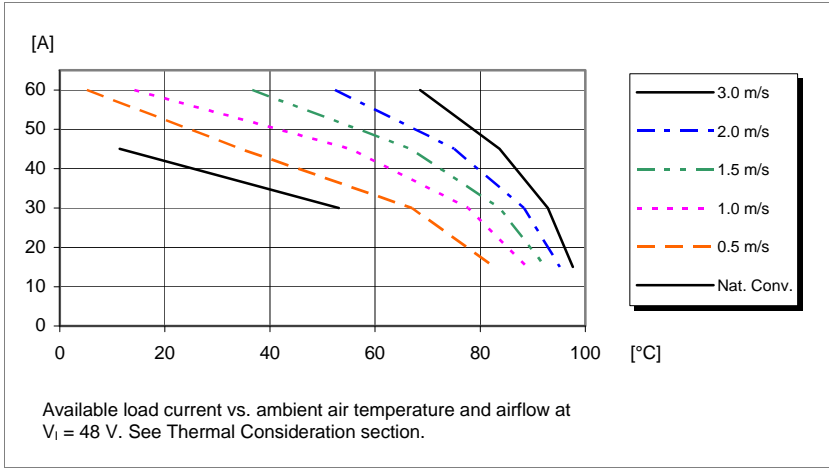
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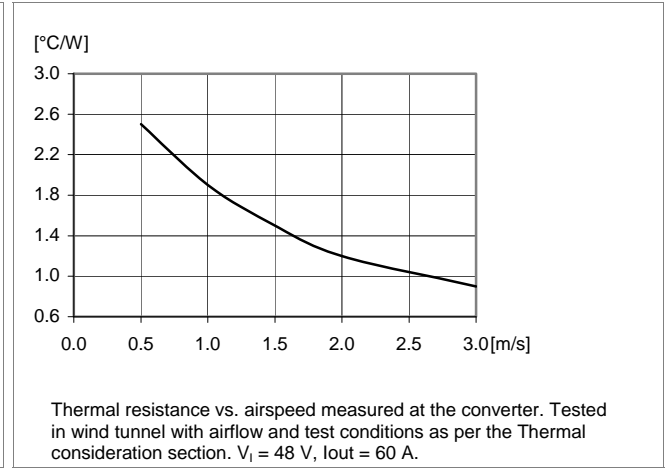
Electrical Specification
12.45 V, 60 A / 711 W

BMR 453 0208/014

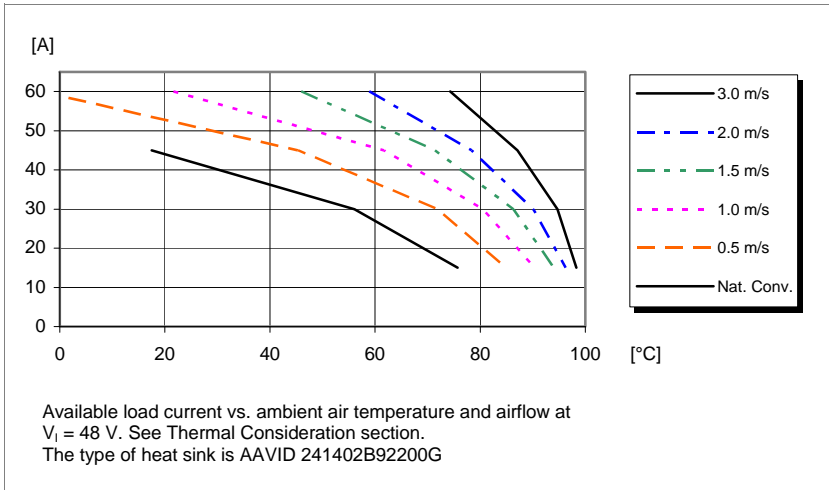
Output Current Derating – Base plate



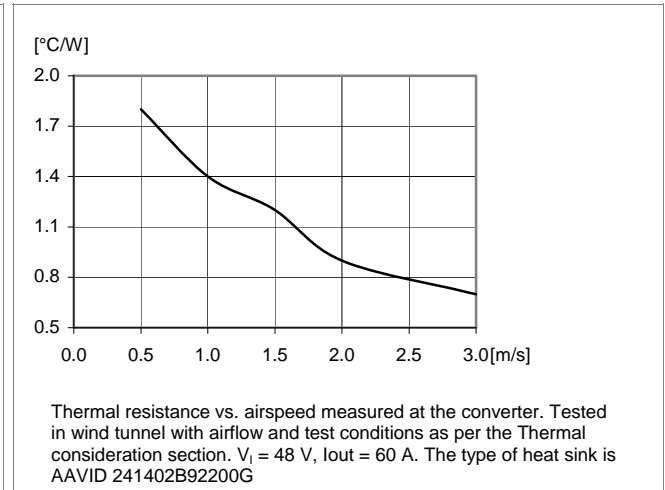
Thermal Resistance – Base plate



Output Current Derating – Base plate with heat sink



Thermal Resistance – Base plate with heat sink



BMR 453 PI series Intermediate Bus Converters
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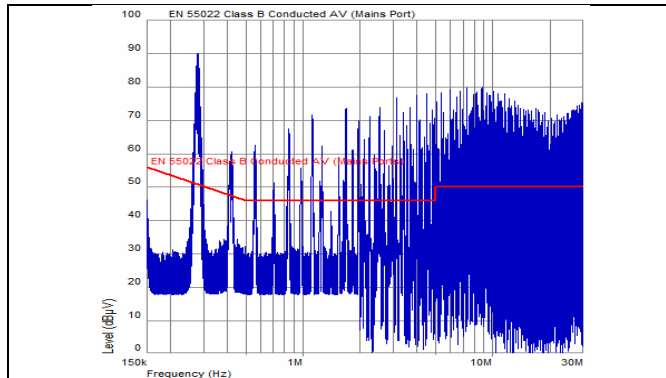
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EMC Specification

Conducted EMI measured according to EN55022, CISPR 22 and FCC part 15J (see test set-up). See Design Note 009 for detailed information. The fundamental switching frequency is 140KHz for BMR 453 at $V_I = 53$ V, max I_O .

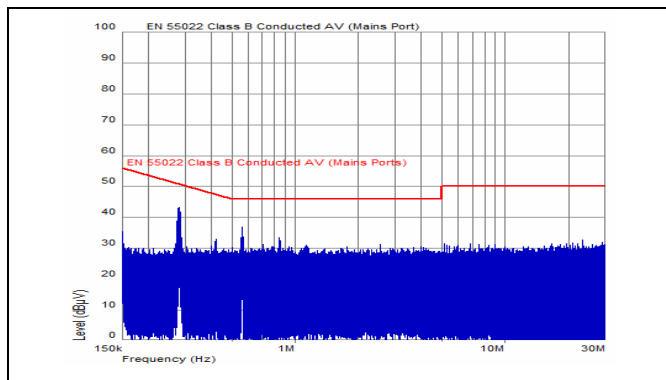
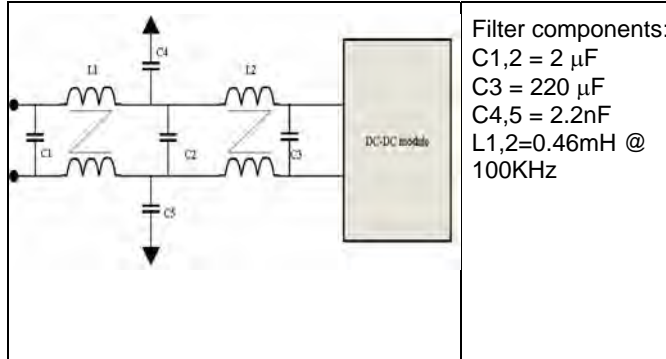
Conducted EMI Input terminal value (typ)



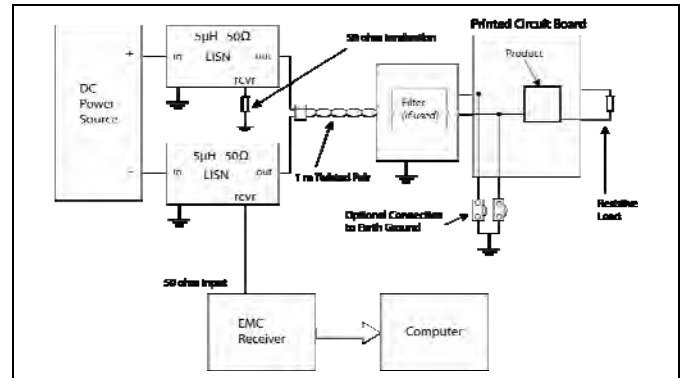
EMI without filter

Optional external filter for class B

Suggested external input filter in order to meet class B in EN 55022, CISPR 22 and FCC part 15J.



EMI with filter



Test set-up

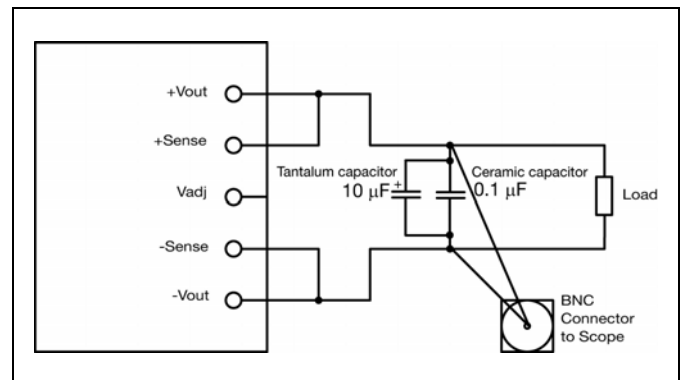
Layout recommendations

The radiated EMI performance of the product will depend on the PWB layout and ground layer design. It is also important to consider the stand-off of the product. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis.

A ground layer will increase the stray capacitance in the PWB and improve the high frequency EMC performance.

Output ripple and noise

Output ripple and noise measured according to figure below. See Design Note 022 for detailed information.



Output ripple and noise test setup

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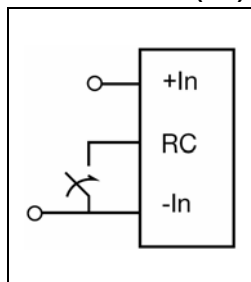
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Operating information
Input Voltage

The input voltage range 45 to 53 Vdc meets the requirements of the European Telecom Standard ETS 300 132-2 for normal input voltage range in -50.0 to -72 V. At input voltages exceeding 75 V, the power loss will be higher than at normal input voltage and T_{P1} must be limited to absolute max +125°C. The absolute maximum continuous input voltage is 80 Vdc.

Turn-off Input Voltage

The product monitors the input voltage and will turn on and turn off at predetermined levels. The minimum hysteresis between turn on and turn off input voltage is 1 V.

Remote Control (RC)


The product is fitted with a remote control function referenced to the primary negative input connection (-In). The RC function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch. The RC pin has an internal pull up resistor to internal voltage reference 18V.

The external device must provide a minimum required sink current to guarantee a maximum voltage on the RC pin (see Electrical characteristics table)

The standard product is provided with "negative logic" RC and will be off until the RC pin is connected to the -In. To turn off the product the RC pin should be left open, or connected to a voltage higher than 13 V referenced to -In. In situations where it is desired to have the product to power up automatically without the need for control signals or a switch, the RC pin can be wired directly to -In.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. The products are designed for stable operation without external capacitors connected to the input or output. The performance in some applications can be enhanced by addition of external capacitance as described under External Decoupling Capacitors. If the input voltage source contains significant inductance, the addition of a 22 - 100 μ F capacitor across the input of the product will ensure stable operation. The capacitor is not required when powering the product from an input source with an inductance below 10 μ H. The minimum required capacitance value depends on the output power and the input voltage. The higher output

power the higher input capacitance is needed.

External Decoupling Capacitors

When powering loads with significant dynamic current requirements, the voltage regulation at the point of load can be improved by addition of decoupling capacitors at the load. The most effective technique is to locate low ESR ceramic and electrolytic capacitors as close to the load as possible, using several parallel capacitors to lower the effective ESR. The ceramic capacitors will handle high-frequency dynamic load changes while the electrolytic capacitors are used to handle low frequency dynamic load changes. Ceramic capacitors will also reduce any high frequency noise at the load. It is equally important to use low resistance and low inductance PWB layouts and cabling. External decoupling capacitors will become part of the product's control loop. The control loop is optimized for a wide range of external capacitance and the maximum recommended value that could be used without any additional analysis is found in the Electrical specification. The ESR of the capacitors is a very important parameter. Stable operation is guaranteed with a verified ESR value of >10 m Ω across the output connections. For further information please contact your local Ericsson Power Modules representative.

Soft-start Power Up

The soft-start control introduces a time-delay (default setting 40 ms) before allowing the output voltage to rise. The default rise time of the ramp up is 10 ms. Power-up is hence completed within 50 ms in default configuration using remote control. When starting by applying input voltage the control circuit boot-up time adds an additional 140 ms delay.

Temperature Protection (OTP)

The product is protected from thermal overload by an internal temperature shutdown protection. When T_{P1} as defined in thermal consideration section is exceeded the product will shut down. The product will make continuous attempts to start up (non-latching mode) and resume normal operation automatically when the temperature has dropped below the temperature threshold. The hysteresis is defined in general electrical specification.

Note: the fault response "continue without interruption" may cause permanent damage of the product.

Over Voltage Protection (OVP)

The product has output over voltage protection that will shut down the product in over voltage conditions.

Over Current Protection (OCP)

The product includes current limiting circuitry for protection at continuous overload. The output voltage will decrease towards zero for output currents in excess of max output

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current (max I_O). The product will resume normal operation after removal of the overload. The load distribution should be designed for the maximum output short circuit current specified.

Fault protection recovery

If one of the two modules exceeds the OVP, OCP or OTP level, the module might turn off depends on its pre-set fault response action, and the other module might not handle more current than its max capability, that will lead to both modules can not recover until the protection trig condition removed, to secure a normal operation, both modules need a reset after the fault condition removed.

Pre-bias Start-up

The product has a Pre-bias start up functionality and will not sink current during start up if a pre-bias source is present at the output terminals.

Input Transient

The products have limited ability to react on sudden input voltage changes. The module can have an output voltage deviation of 2 V when input step is applied (45 V to 53 V). This is tested with a slew rate of 0.1 V/us on the input voltage change and minimum output capacitance 100 uF. Increasing the output capacitance will improve the result.

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Thermal Consideration
General

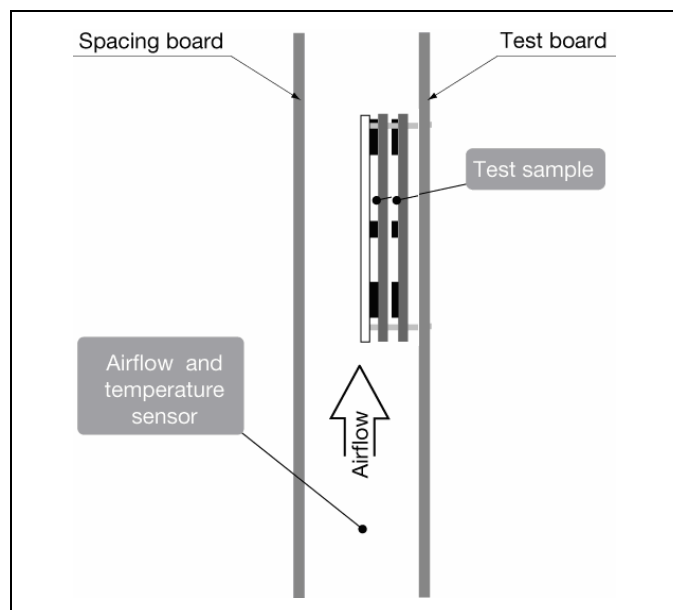
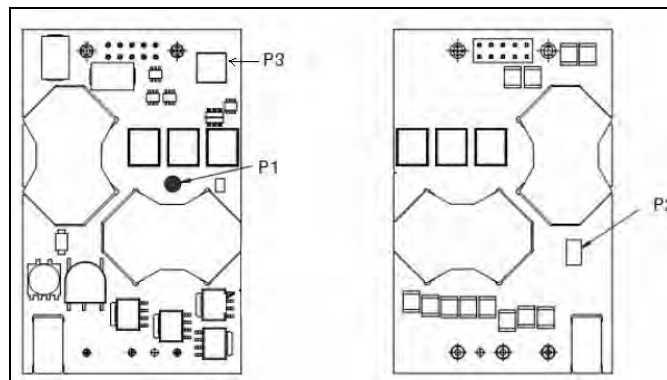
The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation.

For products mounted on a PWB without a heat sink attached, cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependant on the airflow across the product. Increased airflow enhances the cooling of the product. The Output Current Derating graph found in the Output section for each model provides the available output current vs. ambient air temperature and air velocity at $V_I=53V$.

The product is tested on a 254 x 254 mm, 35 μm (1 oz), 16-layer test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm.

measurement points may vary with different thermal design and topology. Temperatures above maximum T_{P1} , measured at the reference point P1 are not allowed and may cause permanent damage.

P1	Upper PCB (close to baseplate) bottom side (away from base plate)	$T_{P1}=125^{\circ}C$
P2	Upper PCB Optical coupler	$T_{P2}=110^{\circ}C$
P3	Lower PCB control IC	$T_{P3}=120^{\circ}C$
P4	Base plate	$T_{P4}=120^{\circ}C$


Definition of product operating temperature under forced air cooling

The product operating temperature is used to monitor the temperature of the product, and proper thermal conditions can be verified by measuring the temperature at positions (P1, P2, P3 and P4). The temperature at these positions (T_{P1} , T_{P2} , T_{P3} , T_{P4}) should not exceed the maximum temperatures in the table below. The number of

Ambient Temperature Calculation

For products with base plate the maximum allowed ambient temperature can be calculated by using the thermal resistance.

1. The power loss is calculated by using the formula $((1/\eta) - 1) \times \text{output power} = \text{power losses (Pd)}$.
 η = efficiency of product. E.g. 95% = 0.95
2. Find the thermal resistance (R_{th}) in the Thermal Resistance graph found in the Output section for each model. **Note that the thermal resistance can be significantly reduced if a heat sink is mounted on the top of the base plate.**

Calculate the temperature increase (ΔT).

$$\Delta T = R_{th} \times P_d$$

3. Max allowed ambient temperature is:

$$\text{Max } T_{P1} - \Delta T.$$

E.g. BMR 453 5100/001 at 2 m/s:

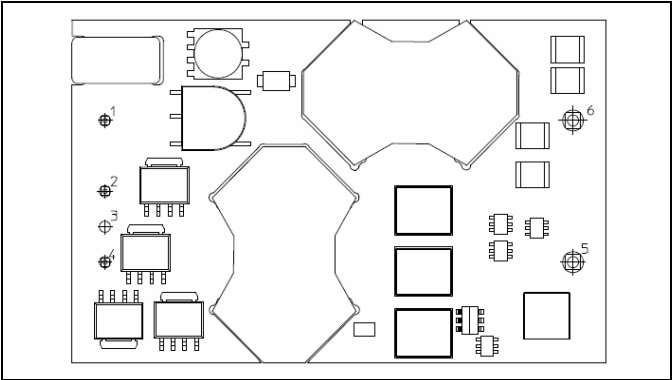
1. $((\frac{1}{0.944}) - 1) \times 396 W = 23.5 W$
2. $23.5 W \times 3.1^{\circ}C/W = 73^{\circ}C$
3. $125^{\circ}C - 73^{\circ}C = \text{max ambient temperature is } 52^{\circ}C$

The actual temperature will be dependent on several factors such as the PWB size, number of layers and direction of airflow.

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Input 44-75 V, Output up to 60 A / 711 W

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Connections (Top view)



Pin	Designation	Function
1	+In	Positive input
2	RC	Remote control
3	Case	Connection to case
4	-In	Negative input
5	-Out	Negative output
6	+Out	Positive output

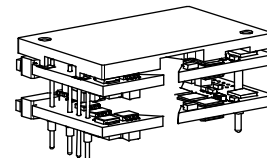
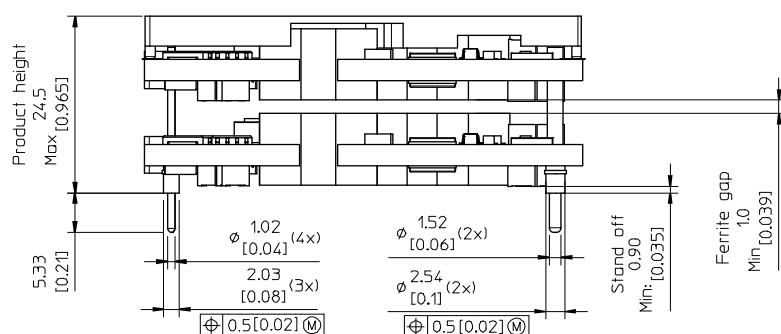
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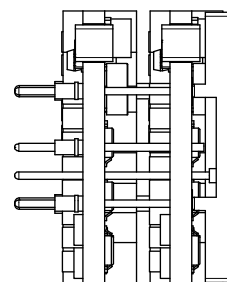
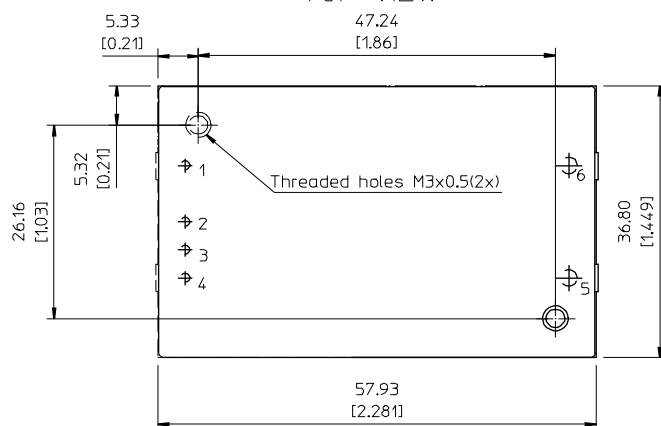
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Mechanical Information – Hole mount – Stacker-Base plate GND version (24.5mm)

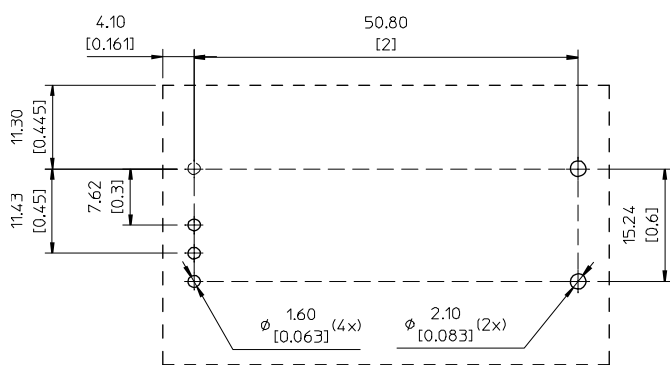
FRONT VIEW



TOP VIEW



RECOMMENDED FOOTPRINT - TOP VIEW



Recommended keep away area for user components

Case:

Material: Aluminium

- For screw attachment apply mounting torque of max 0.44 Nm[3.9 lbf in].
- M3 screws must not protrude more than 2.4 [0.095] into the base plate

Pins:

Material: copper alloy

Plating: 0.1µm Gold over 2µm Nickel

Pin3 is optional and only used for base plate connection

Weight: typical 110 g

All dimensions in mm [inch].

Tolerances unless specified

 x.x mm ±0.50 mm [0.02], x.xx mm ±0.25 mm [0.01]
 (not applied on footprint or typical values)


All component placements – whether shown as physical components or symbolical outline – are for reference only and are subject to change throughout the product's life cycle, unless explicitly described and dimensioned in this drawing.

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Soldering Information – Hole Mounting

The hole mounted product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds.

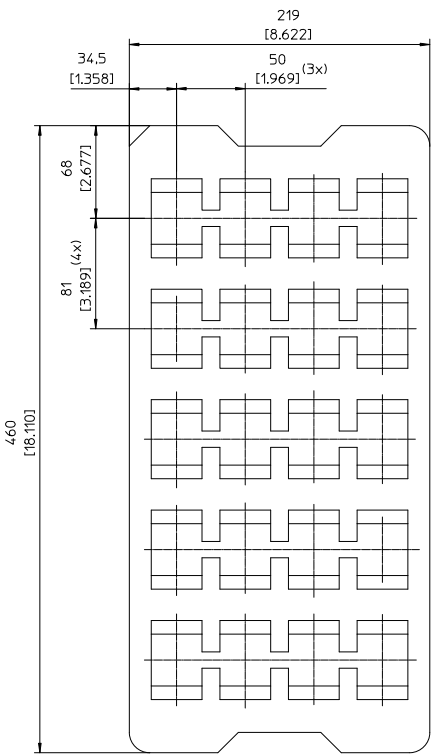
A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

Delivery Package Information – Hole Mount Version

The products are delivered in antistatic trays.

Tray Specifications	
Material	PE Foam
Surface resistance	$10^5 < \text{Ohm/square} < 10^{12}$
Bakability	The trays are not bakeable
Tray capacity	20 converters/tray
Box capacity	20 products (1 full tray/box)
Weight	Product – Stacker option 2460 g full tray, 260 g empty tray



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Product Qualification Specification

Characteristics			
External visual inspection	IPC-A-610		
Change of temperature (Temperature cycling)	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 100°C 1000 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature T _A Duration	-45°C 72 h
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85 % RH 1000 hours
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 h
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Glycol ether Isopropyl alcohol	55°C 35°C 35°C
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Moisture reflow sensitivity ¹	J-STD-020C	Level 1 (SnPb-eutectic) Level 3 (Pb Free)	225°C 260°C
Operational life test	MIL-STD-202G, method 108A	Duration	1000 h
Resistance to soldering heat ²	IEC 60068-2-20 Tb, method 1A	Solder temperature Duration	270°C 10-13 s
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability	IEC 60068-2-58 test Td ¹	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	150°C dry bake 16 h 215°C 235°C
	IEC 60068-2-20 test Ta ²	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	Steam ageing 235°C 245°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g ² /Hz 10 min in each direction

Notes
¹ Only for products intended for reflow soldering (surface mount products)

² Only for products intended for wave soldering (plated through hole products)

BMR454 series Fully regulated Intermediate Bus Converters Input 36-75 V, Output up to 40 A / 240 W	EN/LZT 146 404 R5A July 2011
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Key Features

- Industry standard five pin Eighth-brick
58.4 x 22.7 x 10.2 mm (2.30 x 0.89 x 0.40 in.)
- Optional digital PMBus interface
- Fully regulated intermediate bus converter
- High efficiency, typ. 95.5% at 12 Vout half load
- +/- 2% output voltage tolerance band
- 1500 Vdc input to output isolation
- 2.5 million hours MTBF
- Optional baseplate
- ISO 9001/14001 certified supplier
- PMBus Revision 1.1 compliant



Power Management

- Configurable soft start/stop
- Precision delay and ramp-up
- Voltage sequencing and margining
- Voltage/current/temperature monitoring
- Wide output voltage range
- Configurable protection features
- Synchronization



Safety Approvals



Design for Environment



Meets requirements in high-temperature lead-free soldering processes

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Ordering Information

Product program	Output
BMR4540002/003	3.3 V / 40 A, 132 W
BMR4540002/004	5 V / 38 A, 190 W
BMR4540000/002	9 V / 20 A, 180 W
BMR4540000/001	12 V / 20 A, 240 W (Vin 40-75V)
BMR4540004/005	12 V / 20 A, 240 W (Vin 36-75V)

Product Number and Packaging

BMR454 n ₁ n ₂ n ₃ n ₄ /n ₅ n ₆ n ₇								
Options	n ₁	n ₂	n ₃	n ₄	/	n ₅	n ₆	n ₇
Mechanical pin option	x				/			
Mechanical option		x			/			
Hardware option			x	x	/			
Configuration file					/	x	x	x

Optional designation	Description
n ₁	0 = Standard pin length 5.33 mm 2 = Lead length 3.69 mm (cut) 3 = Lead length 4.57 mm (cut) 4 = Lead length 2.79 mm (cut)
n ₂	0 = Open frame 1 = Baseplate
n ₃ n ₄	00 = 8.1-13.2 Vout with digital interface 01 = 8.1-13.2 Vout without digital interface 02 = 3-6.7 Vout with digital interface 03 = 3-6.7 Vout without digital interface 04 = 12 Vout with digital interface 05 = 12 Vout without digital interface
n ₅ n ₆ n ₇	001 = 12 V Standard configuration (Vin 40-75V, available only for n ₃ n ₄ = 00 or 01) 002 = 9 V Standard configuration 003 = 3.3 V Standard configuration 004 = 5 V Standard configuration 005 = 12 V Standard configuration (Vin 36-75V, available only for n ₃ n ₄ = 04 or 05) 007 = 9 V with positive RC logic configuration 008 = 12 V with positive RC logic configuration (Vin 40-75 V, available only for n ₃ n ₄ = 00 or 01) 009 = 3.3 V with positive RC logic configuration 010 = 5 V with positive RC logic configuration 011 = 12V with positive RC logic configuration (Vin 36-75 V, available only for n ₃ n ₄ = 04 or 05) xxx = Application Specific Configuration
Packaging	25 converters/tray, three (3) trays/box, PE foam dissipative

Example: Product number BMR4542000/002 equals an Through hole mount

lead length 3.69 mm (cut), open frame, digital interface with 9 V standard configuration variant.

For application specific configurations contact your local Ericsson Power Modules sales representative.

General Information
Reliability

The failure rate (λ) and mean time between failures (MTBF = $1/\lambda$) is calculated at max output power and an operating ambient temperature (T_A) of +40°C. Ericsson Power Modules uses Telcordia SR-332 Issue 2 Method 1 to calculate the mean steady-state failure rate and standard deviation (σ).

Telcordia SR-332 Issue 2 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

Mean steady-state failure rate, λ	Std. deviation, σ
394 nFailures/h	61 nFailures/h

MTBF (mean value) for the BMR454 series = 2.5 Mh.
MTBF at 90% confidence level = 2.1 Mh

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2002/95/EC and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Ericsson Power Modules products are found in the Statement of Compliance document.

Ericsson Power Modules fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals (REACH) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of the products.

BMR454 series Fully regulated Intermediate Bus Converters
Input 36-75 V, Output up to 40 A / 240 W

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Warranty

Warranty period and conditions are defined in Ericsson Power Modules General Terms and Conditions of Sale.

Limitation of Liability

Ericsson Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

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Safety Specification**General information**

Ericsson Power Modules DC/DC converters and DC/DC regulators are designed in accordance with safety standards IEC/EN/UL 60950-1 *Safety of Information Technology Equipment*.

IEC/EN/UL 60950-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Energy hazards
- Fire
- Mechanical and heat hazards
- Radiation hazards
- Chemical hazards

On-board DC/DC converters and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without "Conditions of Acceptability". Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use should comply with the requirements in IEC 60950-1, EN 60950-1 and UL 60950-1 *Safety of Information Technology Equipment*. There are other more product related standards, e.g. IEEE 802.3 *CSMA/CD (Ethernet) Access Method*, and ETS-300132-2 *Power supply interface at the input to telecommunications equipment, operated by direct current (dc)*, but all of these standards are based on IEC/EN/UL 60950-1 with regards to safety.

Ericsson Power Modules DC/DC converters and DC/DC regulators are UL 60950-1 recognized and certified in accordance with EN 60950-1.

The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

The products should be installed in the end-use equipment, in accordance with the requirements of the ultimate application. Normally the output of the DC/DC converter is considered as SELV (Safety Extra Low Voltage) and the input source must be isolated by minimum Double or Reinforced Insulation from the primary circuit (AC mains) in accordance with IEC/EN/UL 60950-1.

Isolated DC/DC converters

It is recommended that a slow blow fuse is to be used at the input of each DC/DC converter. If an input filter is used in the circuit the fuse should be placed in front of the input filter.

In the rare event of a component problem that imposes a short circuit on the input source, this fuse will provide the following functions:

- Isolate the fault from the input power source so as not to affect the operation of other parts of the system.
- Protect the distribution wiring from excessive current and power loss thus preventing hazardous overheating.

The galvanic isolation is verified in an electric strength test. The test voltage (V_{iso}) between input and output is 1500 Vdc or 2250 Vdc (refer to product specification).

24 V DC systems

The input voltage to the DC/DC converter is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

48 and 60 V DC systems

If the input voltage to the DC/DC converter is 75 Vdc or less, then the output remains SELV (Safety Extra Low Voltage) under normal and abnormal operating conditions.

Single fault testing in the input power supply circuit should be performed with the DC/DC converter connected to demonstrate that the input voltage does not exceed 75 Vdc.

If the input power source circuit is a DC power system, the source may be treated as a TNV-2 circuit and testing has demonstrated compliance with SELV limits in accordance with IEC/EN/UL60950-1.

Non-isolated DC/DC regulators

The input voltage to the DC/DC regulator is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

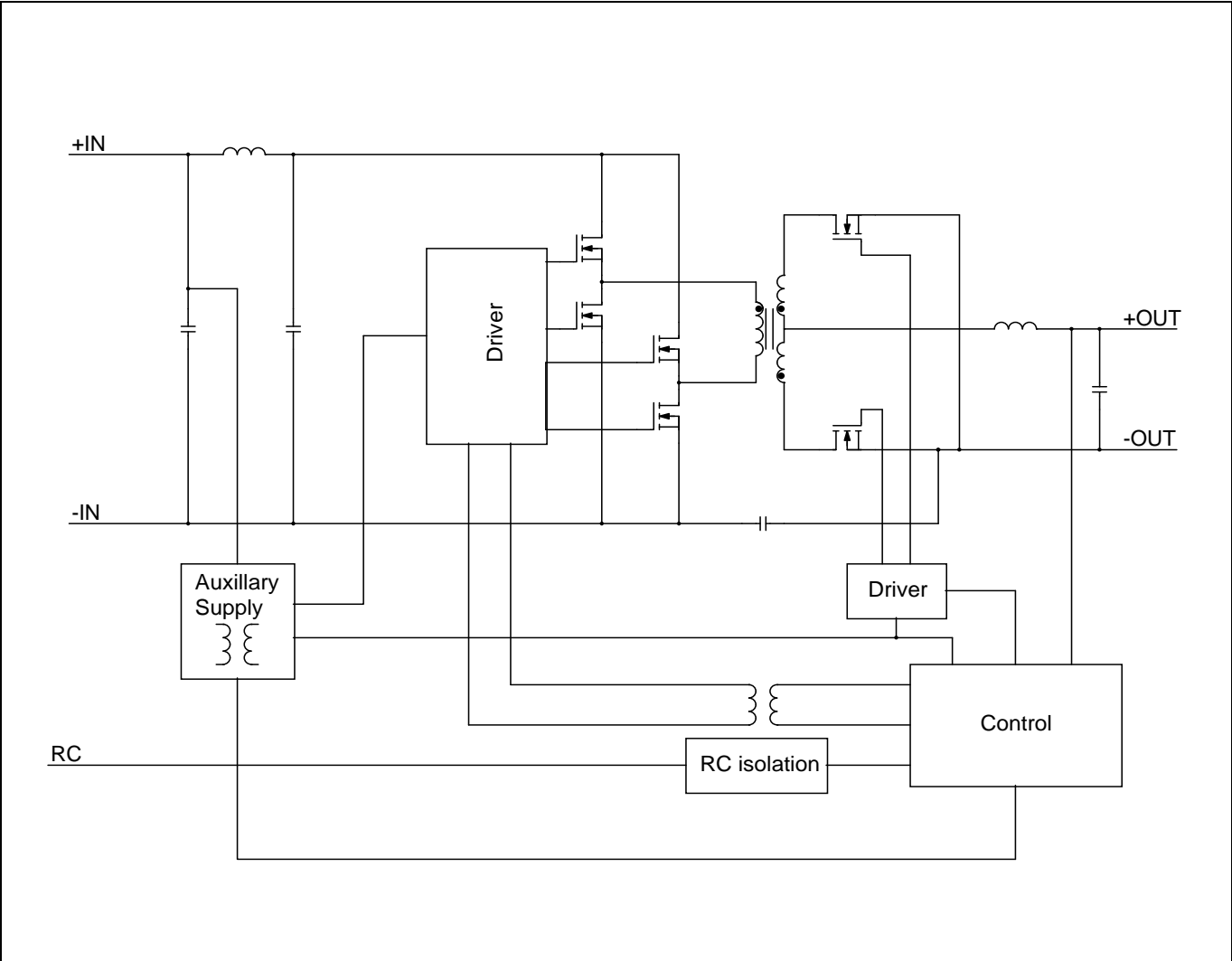
BMR454 series Fully regulated Intermediate Bus Converters Input 36-75 V, Output up to 40 A / 240 W	EN/LZT 146 404 R5A July 2011
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Absolute Maximum Ratings

Characteristics		min	typ	max	Unit
T _{P1}	Operating Temperature (see Thermal Consideration section)	-40		+125	°C
T _S	Storage temperature	-55		+125	°C
V _I	Input voltage	-0.5		80	V
V _{iso}	Isolation voltage (input to output test voltage), see note 1			1500	Vdc
V _{tr}	Input voltage transient (Tp 100 ms)			100	V
V _{RC}	Remote Control pin voltage	-0.3		18	V
V Logic I/O	SALERT, CTRL, SYNC, SCL, SDA, SA(0,1)	-0.3		3.6	V

Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits of Output data or Electrical Characteristics. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.
Note 1: Isolation voltage (input/output to base-plate) max 750 Vdc.

Fundamental Circuit Diagram



BMR454 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 40 A / 240 W

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Functional Description
 $T_{P1} = -40$ to $+90^{\circ}\text{C}$, $V_I = 36$ to 75 V, sense pins connected to output pins unless otherwise specified under Conditions.

 Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, max I_O , unless otherwise specified under Conditions

Configuration File: 190 10-CDA 102 1900/001 rev A

Characteristics		Conditions	min	typ	max	Unit
PMBus monitoring accuracy						
VIN_READ	Input voltage		-3	+0.4	3	%
VOUT_READ	Output voltage	$V_I = 53$ V	-1.0	-0.3	1.0	%
IOUT_READ	Output current	$V_I = 53$ V, 50-100% of max I_O	-6	-1.0	6	%
IOUT_READ	Output current	$V_I = 53$ V, 10% of max I_O	-0.7	-	0.7	A
TEMP_READ	Temperature		-5	-	5	$^{\circ}\text{C}$
Fault Protection Characteristics						
Input Under Voltage Lockout, UVLO	Factory default		-	33	-	V
	Setpoint accuracy		-3	-	3	%
	Hysteresis	Factory default	-	1.8	-	V
		Configurable via PMBus of threshold range, Note 1	0	-	-	V
	Delay		-	200	-	μs
(Output voltage) Over/Under Voltage Protection, OVP/UVLP	VOUT_UV_FAULT_LIMIT	Factory default	-	0	-	V
		Configurable via PMBus, Note 1	0	-	16	V
	VOUT_OV_FAULT_LIMIT	Factory default	-	15.6	-	V
		Configurable via PMBus, Note 1	V_{OUT}	-	16	V
	fault response time		-	200	-	μs
Over Current Protection, OCP	Setpoint accuracy	I_O	-6		6	%
	IOUT_OC_FAULT_LIMIT	Factory default	-	25	-	A
		Configurable via PMBus, Note 1	0	-	100	
	fault response time		-	200	-	μs
Over Temperature Protection, OTP	OTP_FAULT_LIMIT	Factory default	-	125	-	$^{\circ}\text{C}$
		Configurable via PMBus, Note 1	-50		125	
	OTP hysteresis	Factory default		10		
		Configurable via PMBus, Note 1	0		165	
	fault response time		-	200	-	μs
Logic Input/Output Characteristics						
Logic input low (V_{IL})		CTRL_CS, SA0, SA1, PG_SYNC, SCL, SDA,	-	-	0.8	V
Logic input high (V_{IH})			2.0	-	-	V
Logic output low (V_{OL})		CTRL_CS, PG_SYNC, SALERT, SCL, SDA $I_{OL} = 5$ mA	-	-	0.4	V
Logic output high (V_{OH})		CTRL_CS, PG_SYNC, SALERT, SCL, SDA $I_{OH} = -5$ mA	2.8	-	-	V
Setup time, SMBus			100	-		ns
Hold time, SMBus			300	-		ns
Bus free time T(BUF)		Note 2	200	-		us

Note 1: See Operating Information section.

Note 2: It is recommended that a PMBus master read back written data for verification i.e. do not rely on the ACK/NACK bit since this bit are as susceptible to errors as any other bit*. However, under very rare operating conditions, it is possible to get intermittent read back failures. It is therefore recommended to implement error handling in the master that also deals with those situations.

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3.3 V, 40 A / 132 W Electrical Specification
BMR 454 0002/003
 $T_{P1} = -40$ to $+90^{\circ}\text{C}$, $V_I = 36$ to 75 V, sense pins connected to output pins unless otherwise specified under Conditions.

 Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, I_O max, unless otherwise specified under Conditions.

 Additional $C_{out} = 0.1$ mF, Configuration File: 190 10-CDA 102 1900/003 rev A

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage range		36		75	V
V_{loff}	Turn-off input voltage	Decreasing input voltage	32	33	34	V
V_{lon}	Turn-on input voltage	Increasing input voltage	34	35	36	V
C_i	Internal input capacitance			11		μF
P_O	Output power		0		132	W
η	Efficiency	50% of max I_O		93		%
		max I_O		91.2		
		50% of max I_O , $V_I = 48$ V		93.2		
		max I_O , $V_I = 48$ V		91.2		
P_d	Power Dissipation	max I_O		12.8	17.5	W
P_{li}	Input idling power	$I_O = 0$ A, $V_I = 53$ V		2.0		W
P_{RC}	Input standby power	$V_I = 53$ V (turned off with RC)		127		mW
f_s	Switching frequency	0-100 % of max I_O see Note 1	171	180	189	kHz

V_{Oi}	Output voltage initial setting and accuracy	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, $I_O = 40$ A	3.26	3.3	3.34	V
V_O	Output adjust range	See operating information	3.0		6.7	V
	Output voltage tolerance band	0-100% of max I_O	3.22		3.38	V
	Line regulation	max I_O		5	20	mV
	Load regulation	$V_I = 53$ V, 0-100 % of max I_O		6	16	mV
V_{tr}	Load transient voltage deviation	$V_I = 53$ V, Load step 25-75-25% of max I_O , $di/dt = 1$ A/ μs see Note 2		± 0.2		V
t_{tr}	Load transient recovery time			214		μs
t_r	Ramp-up time (from 10-90% of V_{Oi})	10-100% of max I_O , $T_{P1} = 25^{\circ}\text{C}$, $V_I = 53$ V see Note 3		8		ms
t_s	Start-up time (from V_I connection to 90% of V_{Oi})			140		ms
t_f	V_I shut-down fall time (from V_I off to 10% of V_O)	max I_O		0.33		ms
		$I_O = 0$ A		3.8		s
t_{RC}	RC start-up time	max I_O		54		ms
	RC shut-down fall time (from RC off to 10% of V_O)	max I_O		2		ms
		$I_O = 0$ A		3.8		s
I_O	Output current		0		40	A
I_{lim}	Current limit threshold	$V_O = 3.0$ V, $T_{P1} < \text{max } T_{ref}$	41	45	49	A
I_{sc}	Short circuit current	$T_{P1} = 25^{\circ}\text{C}$, $V_O < 0.2$ V, see Note 4		7	8	A
C_{out}	Recommended Capacitive Load	$T_{P1} = 25^{\circ}\text{C}$, see Note 5	0.1	4	6	mF
V_{Oac}	Output ripple & noise	See ripple & noise section, max I_O , V_{Oi}		25	50	mVp-p
OVP	Over voltage protection	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, 10-100% of max I_O , see Note 6		4.6		V

Note 1: Frequency may be adjusted via PMBus, see Operating Information section.

 Note 2: $C_{out} = 4$ mF used at load transient test.

Note 3: Start-up and Ramp-up time can be increased via PMBus, see Operation Information section.

Note 4: RMS current in hiccup mode.

Note 5: Low ESR-value.

Note 6: OVP-level can be adjusted via PMBus, see Operation Information section.

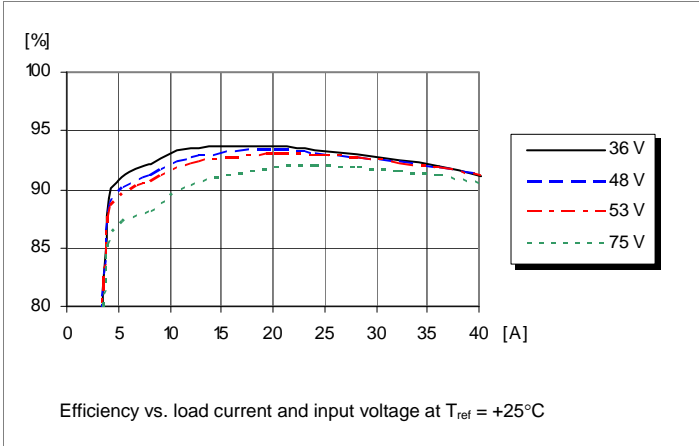
BMR454 series Fully regulated Intermediate Bus Converters
Input 36-75 V, Output up to 40 A / 240 W

EN/LZT 146 404 R5A July 2011
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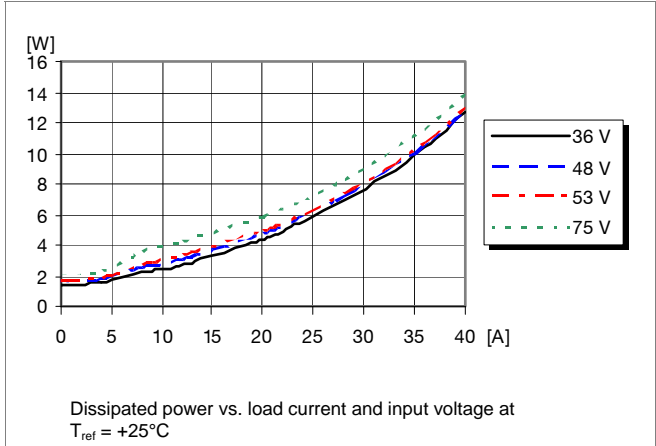
3.3 V, 40 A / 132 W Electrical Specification

BMR 454 0002/003

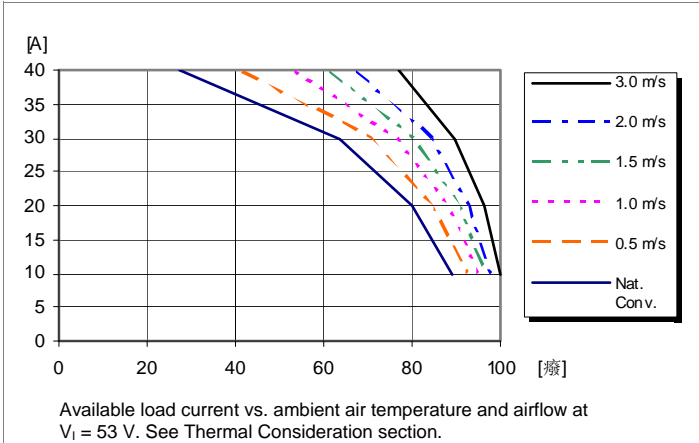
Efficiency



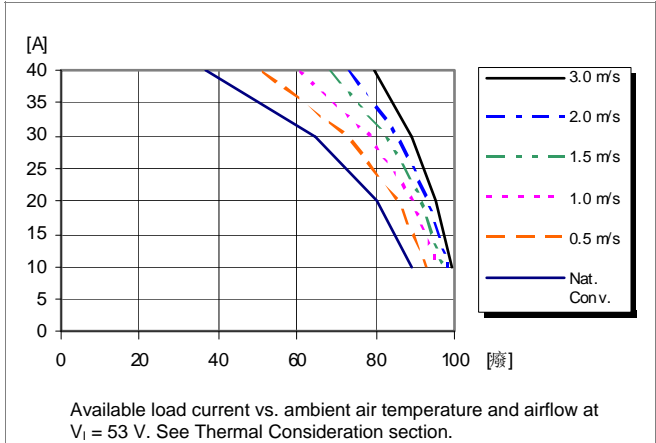
Power Dissipation



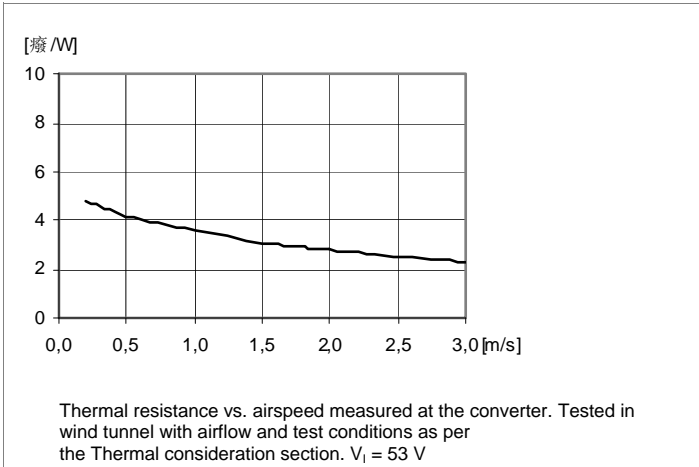
Output Current Derating, open frame



Output Current Derating, base plate option



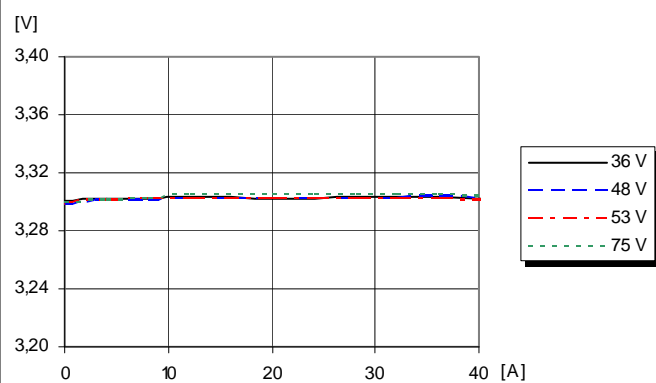
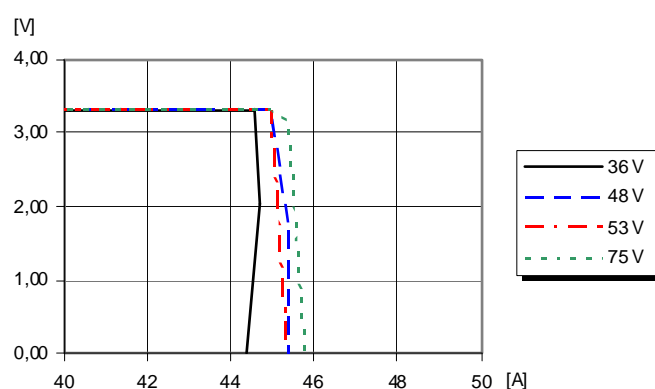
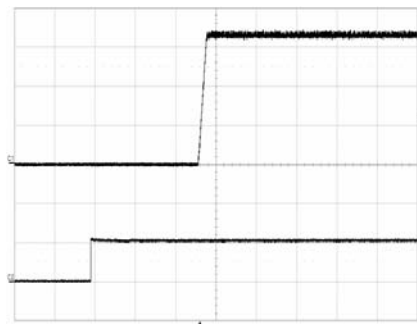
Thermal Resistance, base plate option



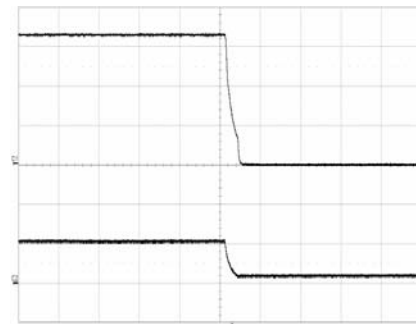
BMR454 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 40 A / 240 W

EN/LZT 146 404 R5A July 2011

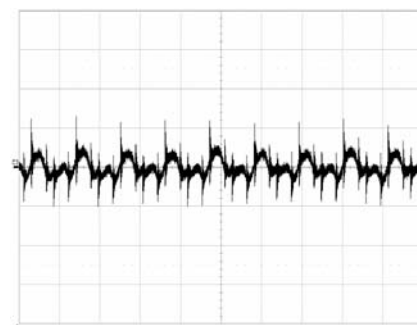
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3.3 V, 40 A / 132 W Electrical Specification
BMR 454 0002/003
Output Characteristics

 Output voltage vs. load current at $T_{ref} = +25^{\circ}\text{C}$
Current Limit Characteristics

 Output voltage vs. load current at $I_O > \max I_O$, $T_{ref} = +25^{\circ}\text{C}$
Start-up

 Start-up enabled by connecting V_I at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 40\text{ A}$ resistive load.

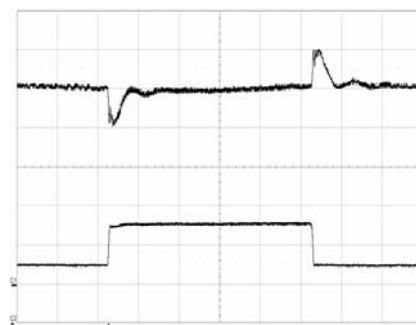
 Top trace: output voltage (1 V/div.).
 Bottom trace: input voltage (50 V/div.).
 Time scale: (50 ms/div.).

Shut-down

 Shut-down enabled by disconnecting V_I at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 40\text{ A}$ resistive load.

 Top trace: output voltage (2 V/div.).
 Bottom trace: input voltage (50 V/div.).
 Time scale: (0.5 ms/div.).

Output Ripple & Noise

 Output voltage ripple at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 40\text{ A}$ resistive load.

 Trace: output voltage (10 mV/div.).
 Time scale: (5 μs /div.).

Output Load Transient Response

 Output voltage response to load current step-
 change (10 - 30 - 10 A) at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$, $C_O = 4\text{ mF}$

 Top trace: output voltage (0.2 V/div.).
 Bottom trace: output current (20 A/div.).
 Time scale: (0.5 ms/div.).

BMR454 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 40 A / 240 W

EN/LZT 146 404 R5A July 2011

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5 V, 38 A / 190 W Electrical Specification
BMR 454 0002/004
 $T_{P1} = -40$ to $+90^{\circ}\text{C}$, $V_I = 36$ to 75 V, sense pins connected to output pins unless otherwise specified under Conditions.

 Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, I_O max, unless otherwise specified under Conditions.

 Additional $C_{out} = 0.1$ mF, Configuration File: 190 10-CDA 102 1900/004 rev A

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage range		36		75	V
V_{loff}	Turn-off input voltage	Decreasing input voltage	32	33	34	V
V_{lon}	Turn-on input voltage	Increasing input voltage	34	35	36	V
C_i	Internal input capacitance			11		μF
P_O	Output power		0		190	W
η	Efficiency	50% of max I_O		94.3		%
		max I_O		93.3		
		50% of max I_O , $V_I = 48$ V		94.5		
		max I_O , $V_I = 48$ V		93.3		
P_d	Power Dissipation	max I_O		13.7	19.1	W
P_{li}	Input idling power	$I_O = 0$ A, $V_I = 53$ V		2.6		W
P_{RC}	Input standby power	$V_I = 53$ V (turned off with RC)		123		mW
f_s	Switching frequency	0-100% of max I_O see Note 1	171	180	189	kHz

V_{Oi}	Output voltage initial setting and accuracy	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, $I_O = 38$ A	4.95	5.0	5.05	V
V_O	Output adjust range	See operating information	3.0		6.7	V
	Output voltage tolerance band	0-100% of max I_O	4.9		5.1	V
	Line regulation	max I_O		5	21	mV
	Load regulation	$V_I = 53$ V, 0-100% of max I_O		5	18	mV
V_{tr}	Load transient voltage deviation	$V_I = 53$ V, Load step 25-75-25% of max I_O , $di/dt = 1$ A/ μs see Note 2		± 0.2		V
t_{tr}	Load transient recovery time			250		μs
t_r	Ramp-up time (from 10-90% of V_{Oi})	10-100% of max I_O , $T_{P1} = 25^{\circ}\text{C}$, $V_I = 53$ V see Note 3		8		ms
t_s	Start-up time (from V_I connection to 90% of V_{Oi})			140		ms
t_f	V_I shut-down fall time (from V_I off to 10% of V_O)	max I_O		0.4		ms
		$I_O = 0$ A		3.7		s
t_{RC}	RC start-up time	max I_O		55		ms
	RC shut-down fall time (from RC off to 10 % of V_O)	max I_O		3		ms
		$I_O = 0$ A		3.7		s
I_O	Output current		0		38	A
I_{lim}	Current limit threshold	$V_O = 4.5$ V, $T_{P1} < \text{max } T_{ref}$	41	45	49	A
I_{sc}	Short circuit current	$T_{P1} = 25^{\circ}\text{C}$, $V_O < 0.2$ V, see Note 4		7	8	A
C_{out}	Recommended Capacitive Load	$T_{P1} = 25^{\circ}\text{C}$, see Note 5	0.1	3.8	6	mF
V_{Oac}	Output ripple & noise	See ripple & noise section, max I_O , V_{Oi}		35	75	mVp-p
OVP	Over voltage protection	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, 10-100% of max I_O , see Note 6		6.8		V

Note 1: Frequency may be adjusted via PMBus, see Operating Information section.

 Note 2: $C_{out} = 3.8$ mF used at load transient test.

Note 3: Start-up and Ramp-up time can be increased via PMBus, see Operation Information section.

Note 4: RMS current in hiccup mode.

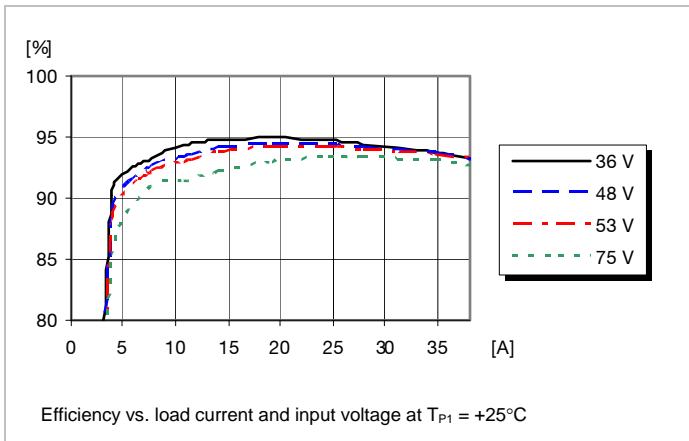
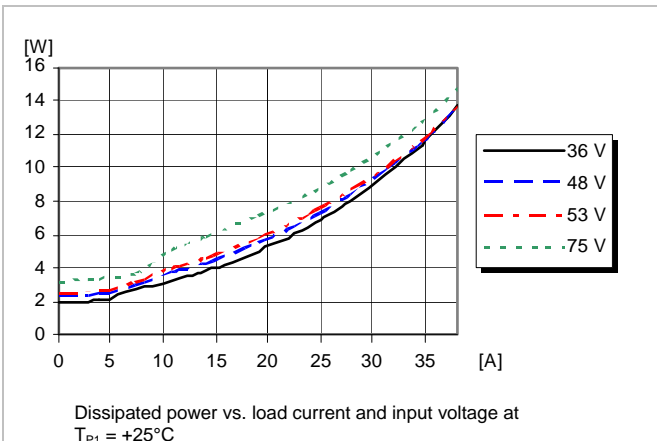
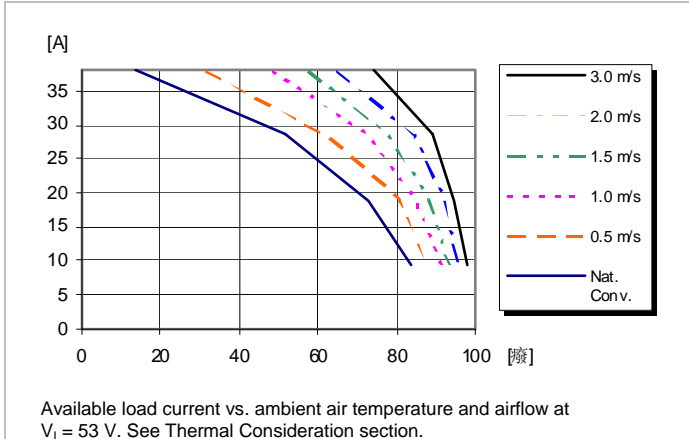
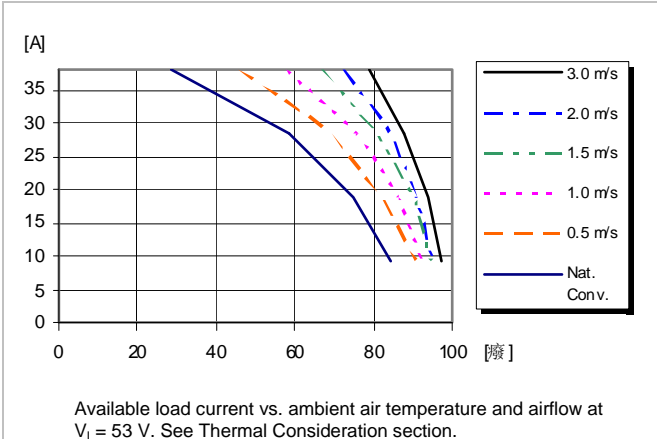
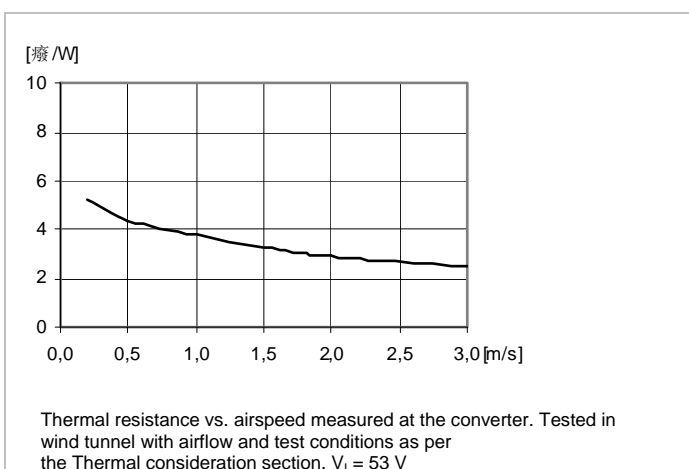
Note 5: Low ESR-value.

Note 6: OVP-level can be adjusted via PMBus, see Operation Information section.

BMR454 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 40 A / 240 W

EN/LZT 146 404 R5A July 2011

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5 V, 38 A / 190 W Electrical Specification
BMR 454 0002/004
Efficiency

Power Dissipation

Output Current Derating, open frame

Output Current Derating, base plate option

Thermal Resistance, base plate option


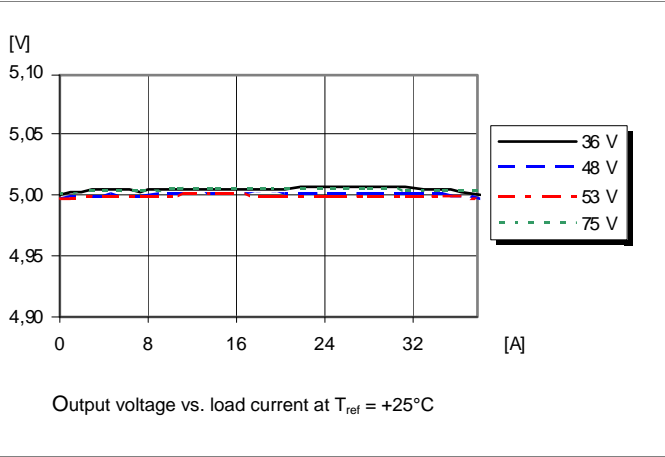
BMR454 series Fully regulated Intermediate Bus Converters
Input 36-75 V, Output up to 40 A / 240 W

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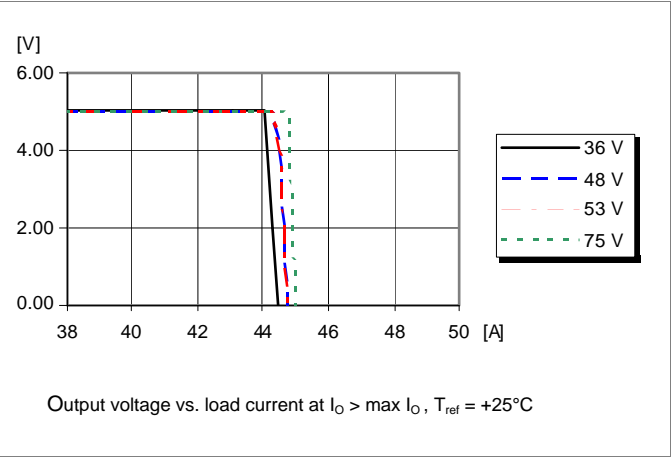
5 V, 38 A / 190 W Electrical Specification

BMR 454 0002/004

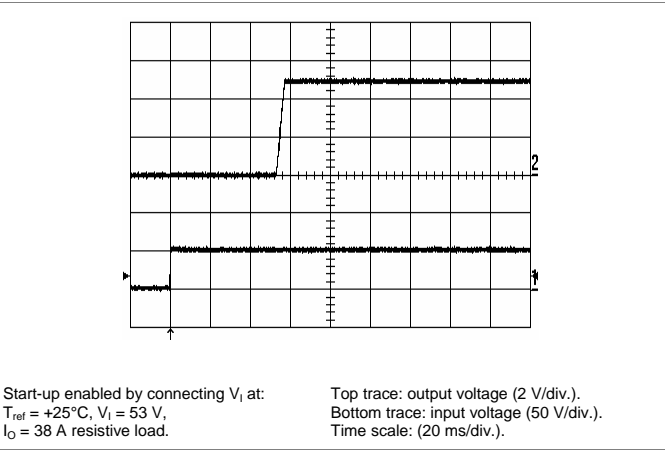
Output Characteristics



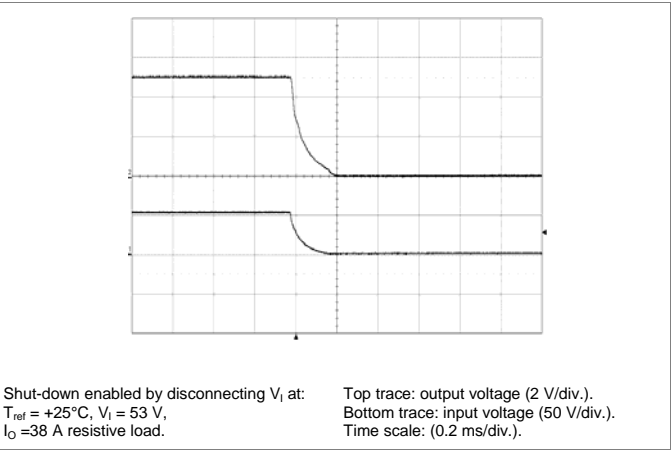
Current Limit Characteristics



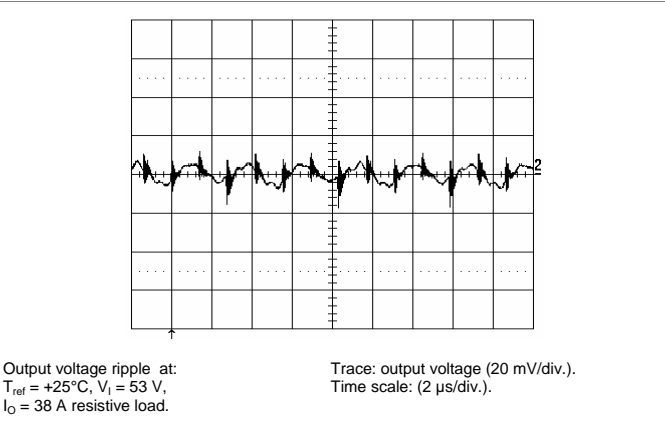
Start-up



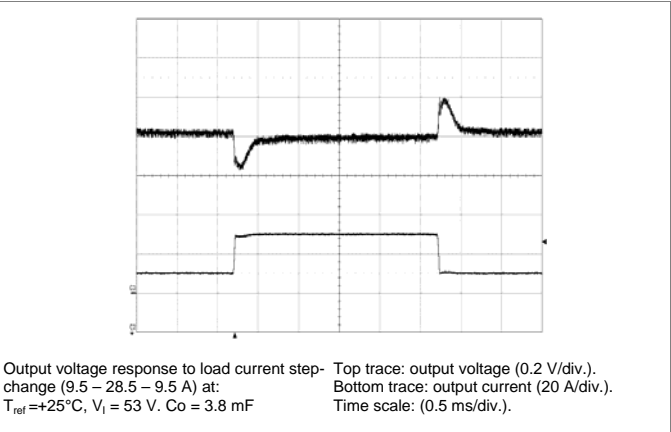
Shut-down



Output Ripple & Noise



Output Load Transient Response



BMR454 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 40 A / 240 W

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9 V, 20 A / 180 W Electrical Specification
BMR 454 0000/002
 $T_{P1} = -40$ to $+90^{\circ}\text{C}$, $V_I = 36$ to 75 V, sense pins connected to output pins unless otherwise specified under Conditions.

 Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, I_O max, unless otherwise specified under Conditions.

 Additional $C_{out} = 0.1$ mF, Configuration File: 190 10-CDA 102 1900/002 rev A

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage range		36		75	V
V_{loff}	Turn-off input voltage	Decreasing input voltage	32	33	34	V
V_{lon}	Turn-on input voltage	Increasing input voltage	34	35	36	V
C_I	Internal input capacitance			11		μF
P_O	Output power		0		180	W
η	Efficiency	50% of max I_O		95		%
		max I_O		94		
		50% of max I_O , $V_I = 48$ V		95		
		max I_O , $V_I = 48$ V		94		
P_d	Power Dissipation	max I_O		11.1	14.7	W
P_{li}	Input idling power	$I_O = 0$ A, $V_I = 53$ V		2.2		W
P_{RC}	Input standby power	$V_I = 53$ V (turned off with RC)		182		mW
f_s	Switching frequency	0-100% of max I_O see Note 1	171	180	189	kHz

V_{Oi}	Output voltage initial setting and accuracy	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, $I_O = 20$ A	8.90	9.0	9.10	V
V_O	Output adjust range	See operating information	8.1		13.2	V
	Output voltage tolerance band	0-100% of max I_O	8.82		9.18	V
	Line regulation	max I_O		8	45	mV
	Load regulation	$V_I = 53$ V, 0-100% of max I_O		8	30	mV
V_{tr}	Load transient voltage deviation	$V_I = 53$ V, Load step 25-75-25% of max I_O , $di/dt = 1$ A/ μs see Note 2		± 0.3		V
t_{tr}	Load transient recovery time			250		μs
t_r	Ramp-up time (from 10-90% of V_{Oi})	10-100% of max I_O , $T_{P1} = 25^{\circ}\text{C}$, $V_I = 53$ V see Note 3		10		ms
t_s	Start-up time (from V_I connection to 90% of V_{Oi})			140		ms
t_f	V_I shut-down fall time (from V_I off to 10% of V_O)	max I_O		0.4		ms
		$I_O = 0$ A		5		s
t_{RC}	RC start-up time	max I_O		54		ms
	RC shut-down fall time (from RC off to 10% of V_O)	max I_O		3		ms
		$I_O = 0$ A		5		s
I_O	Output current		0		20	A
I_{lim}	Current limit threshold	$V_O = 8.1$ V, $T_{P1} < \text{max } T_{ref}$	21	25	28	A
I_{sc}	Short circuit current	$T_{P1} = 25^{\circ}\text{C}$, $V_O < 0.2$ V, see Note 4		4	5	A
C_{out}	Recommended Capacitive Load	$T_{P1} = 25^{\circ}\text{C}$, see Note 5	0.1	2.2	6	mF
V_{Oac}	Output ripple & noise	See ripple & noise section, max I_O , V_{Oi}		60	120	mVp-p
OVP	Over voltage protection	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, 10-100% of max I_O , see Note 6		15.6		V

Note 1: Frequency may be adjusted via PMBus, see Operating Information section.

 Note 2: $C_{out} = 3.3$ mF used at load transient test.

Note 3: Start-up and Ramp-up time can be increased via PMBus, see Operation Information section.

Note 4: RMS current in hiccup mode.

Note 5: Low ESR-value.

Note 6: OVP-level can be adjusted via PMBus, see Operation Information section.

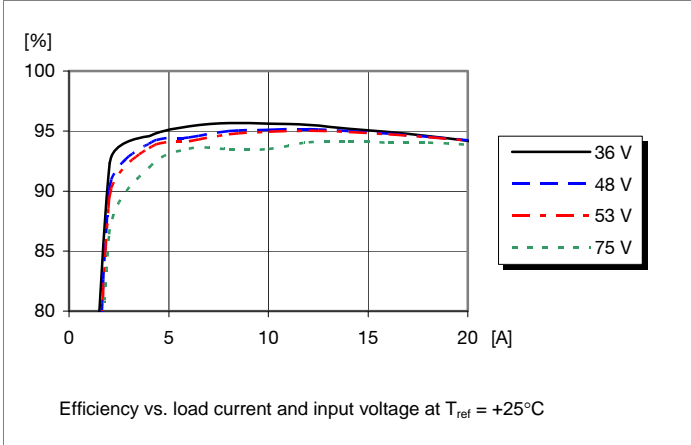
BMR454 series Fully regulated Intermediate Bus Converters
Input 36-75 V, Output up to 40 A / 240 W

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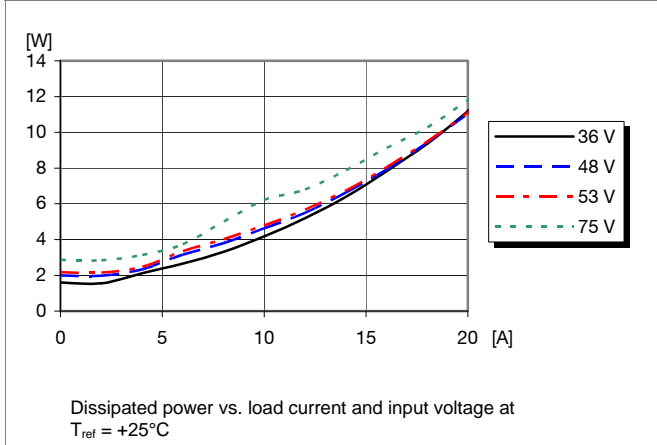
9 V, 20 A / 180 W Electrical Specification

BMR 454 0000/002

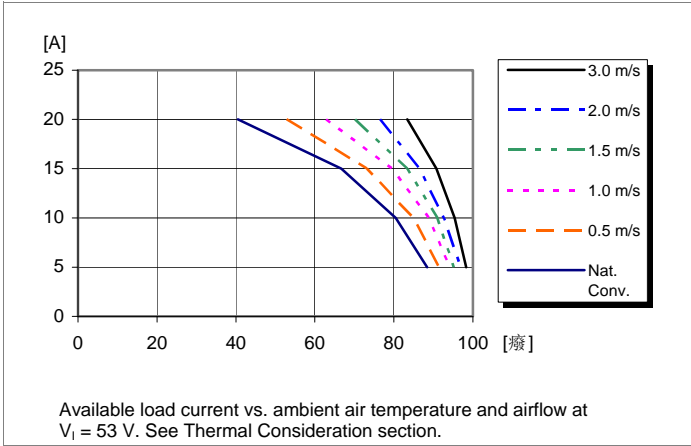
Efficiency



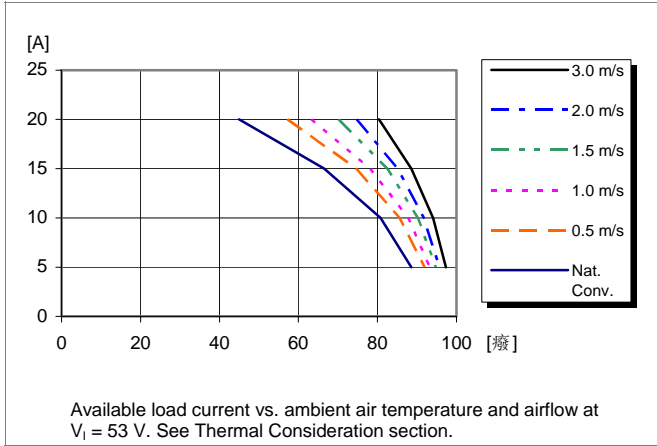
Power Dissipation



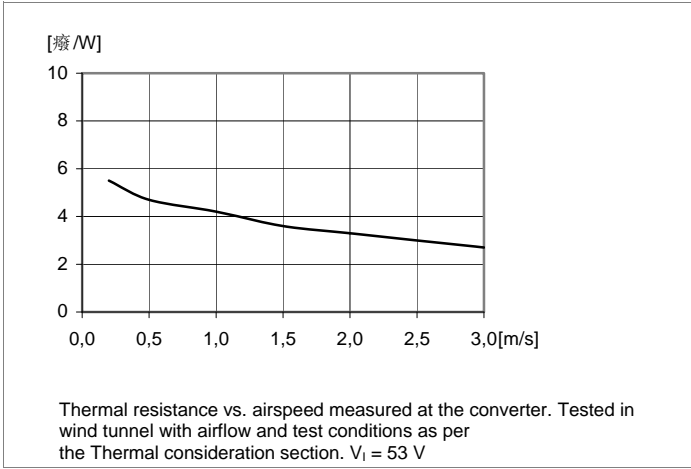
Output Current Derating, open frame



Output Current Derating, base plate option



Thermal Resistance, base plate option



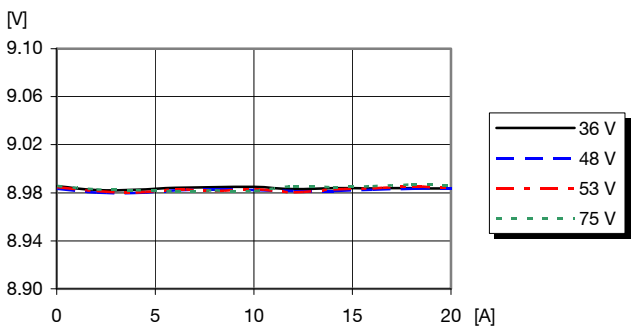
BMR454 series Fully regulated Intermediate Bus Converters
Input 36-75 V, Output up to 40 A / 240 W

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9 V, 20 A / 180 W Electrical Specification

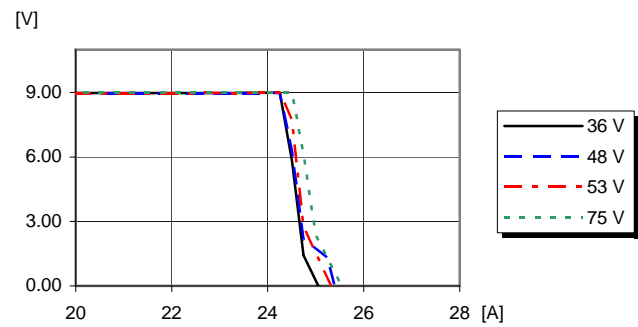
BMR 454 0000/002

Output Characteristics



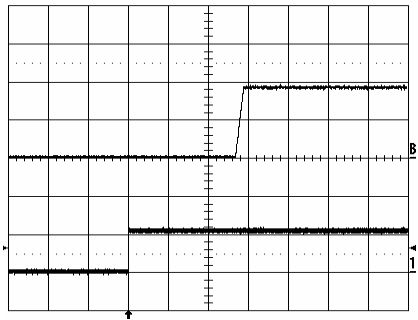
Output voltage vs. load current at $T_{ref} = +25^{\circ}\text{C}$

Current Limit Characteristics



Output voltage vs. load current at $I_O > \max I_O$, $T_{ref} = +25^{\circ}\text{C}$

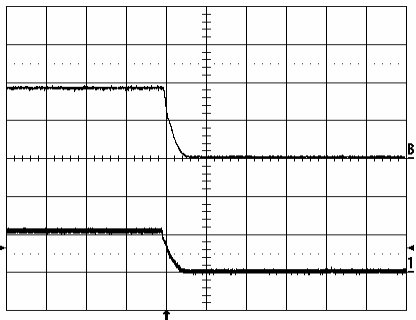
Start-up



Start-up enabled by connecting V_I at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 20\text{ A}$ resistive load.

Top trace: output voltage (5 V/div.).
Bottom trace: input voltage (50 V/div.).
Time scale: (50 ms/div.).

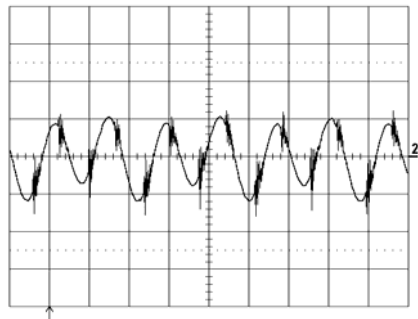
Shut-down



Shut-down enabled by disconnecting V_I at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 20\text{ A}$ resistive load.

Top trace: output voltage (5 V/div.).
Bottom trace: input voltage (50 V/div.).
Time scale: (0.5 ms/div.).

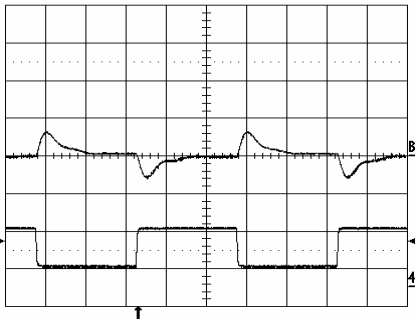
Output Ripple & Noise



Output voltage ripple at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 20\text{ A}$ resistive load.

Trace: output voltage (20 mV/div.).
Time scale: (2 μs/div.).

Output Load Transient Response



Output voltage response to load current step-
change (5 - 15 - 5 A) at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$, $C_O = 2.2\text{ mF}$

Top trace: output voltage (0.5 V/div.).
Bottom trace: output current (10 A/div.).
Time scale: (0.5 ms/div.).

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 Input 36-75 V, Output up to 40 A / 240 W

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12 V, 20 A / 240 W Electrical Specification
BMR 454 0000/001
 $T_{P1} = -40$ to $+90^{\circ}\text{C}$, $V_I = 40$ to 75 V, sense pins connected to output pins unless otherwise specified under Conditions.

 Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, I_O max, unless otherwise specified under Conditions.

 Additional $C_{out} = 0.1$ mF, Configuration File: 190 10-CDA 102 1900/001 rev A

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage range		40		75	V
V_{loff}	Turn-off input voltage	Decreasing input voltage	32	33	34	V
V_{lon}	Turn-on input voltage	Increasing input voltage	34	35	36	V
C_I	Internal input capacitance			11		μF
P_O	Output power		0		240	W
η	Efficiency	50% of max I_O		95.6		%
		max I_O		95.0		
		50% of max I_O , $V_I = 48$ V		95.7		
		max I_O , $V_I = 48$ V		95.0		
P_d	Power Dissipation	max I_O		12.7	17.1	W
P_{li}	Input idling power	$I_O = 0$ A, $V_I = 53$ V		2.7		W
P_{RC}	Input standby power	$V_I = 53$ V (turned off with RC)		184		mW
f_s	Switching frequency	0-100% of max I_O see Note 1	171	180	189	kHz

V_{Oi}	Output voltage initial setting and accuracy	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, $I_O = 20$ A	11.88	12.0	12.12	V
V_O	Output adjust range	See operating information	8.1		13.2	V
	Output voltage tolerance band	0-100% of max I_O	11.76		12.24	V
	Line regulation	max I_O		20	80	mV
	Load regulation	$V_I = 53$ V, 0-100% of max I_O		6	45	mV
V_{tr}	Load transient voltage deviation	$V_I = 53$ V, Load step 25-75-25% of max I_O , $di/dt = 1$ A/ μs see Note 2		± 0.3		V
t_{tr}	Load transient recovery time			250		μs
t_r	Ramp-up time (from 10-90% of V_{Oi})	10-100% of max I_O , $T_{P1} = 25^{\circ}\text{C}$, $V_I = 53$ V see Note 3		8		ms
t_s	Start-up time (from V_I connection to 90% of V_{Oi})			140		ms
t_f	V_I shut-down fall time (from V_I off to 10% of V_O)	max I_O		0.4		ms
		$I_O = 0$ A		5		s
t_{RC}	RC start-up time	max I_O		55		ms
	RC shut-down fall time (from RC off to 10% of V_O)	max I_O		2.4		ms
		$I_O = 0$ A		5		s
I_O	Output current		0		20	A
I_{lim}	Current limit threshold	$V_O = 10.8$ V, $T_{P1} < \max T_{ref}$	21	25	28	A
I_{sc}	Short circuit current	$T_{P1} = 25^{\circ}\text{C}$, see Note 4		4	5	A
C_{out}	Recommended Capacitive Load	$T_{P1} = 25^{\circ}\text{C}$, see Note 5	0.1	2.2	6	mF
V_{Oac}	Output ripple & noise	See ripple & noise section, max I_O		60	120	mVp-p
OVP	Over voltage protection	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, 10-100% of max I_O , see Note 6		15.6		V

Note 1: Frequency may be adjusted with PMBus communication. See Operating Information section

 Note 2: $C_{out} = 2.2$ mF used at load transient test.

Note 3: Start-up and Ramp-up time can be increased via PMBus, see Operation Information section.

Note 4: OCP in hiccup mode

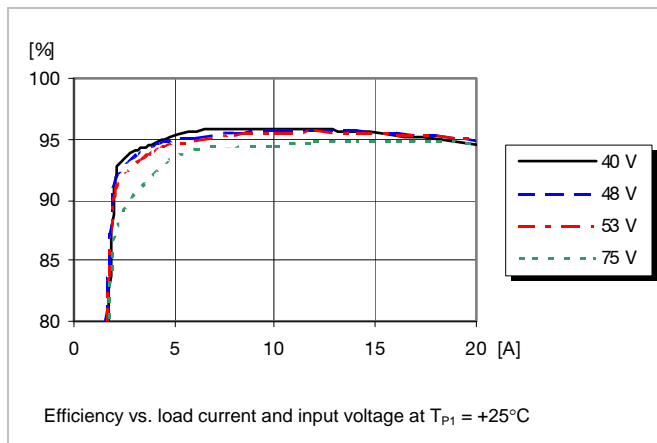
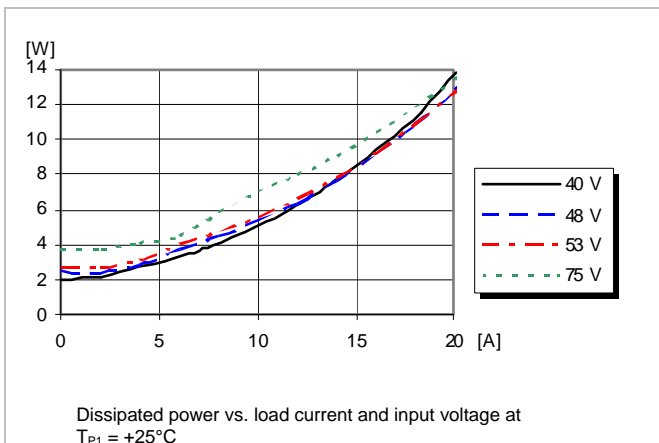
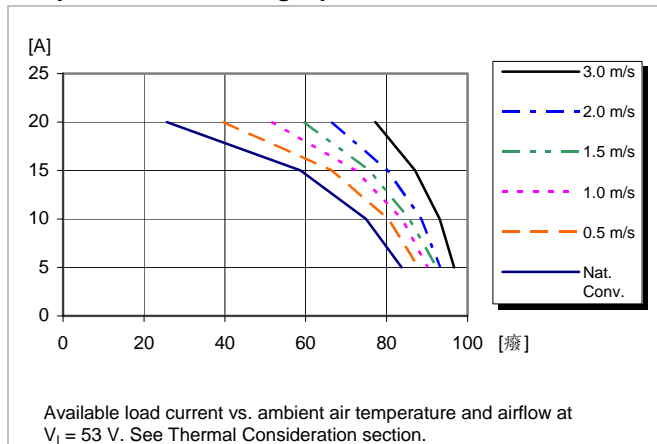
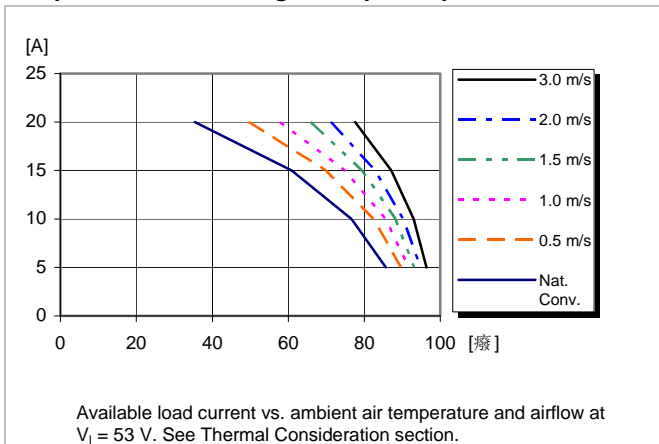
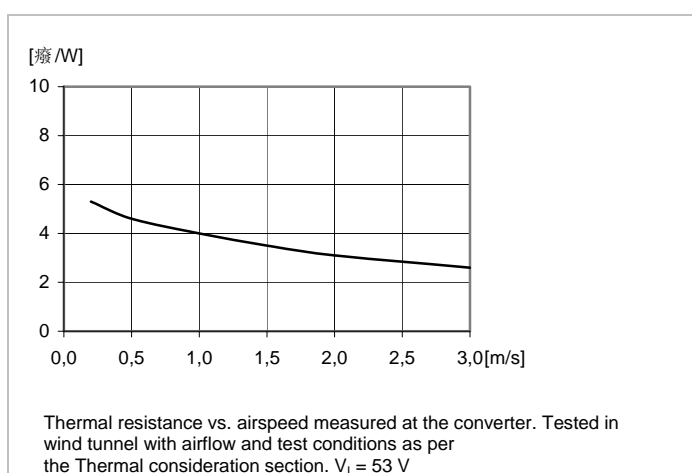
Note 5: Low ESR-value

Note 6: OVP-level can be adjusted via PMBus, see Operation Information section.

BMR454 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 40 A / 240 W

EN/LZT 146 404 R5A July 2011

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12 V, 20 A / 240 W Typical Characteristics
BMR 454 0000/001
Efficiency

Power Dissipation

Output Current Derating, open frame

Output Current Derating, base plate option

Thermal Resistance, base plate option


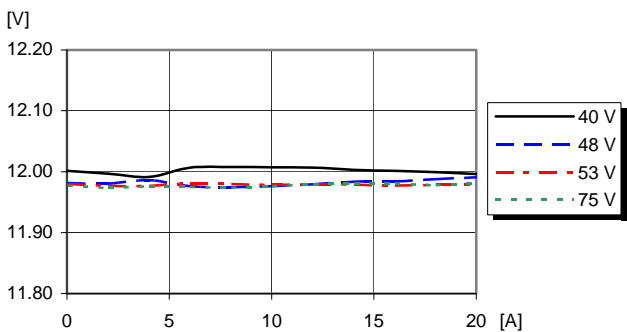
BMR454 series Fully regulated Intermediate Bus Converters
Input 36-75 V, Output up to 40 A / 240 W

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12 V, 20 A / 240 W Electrical Specification

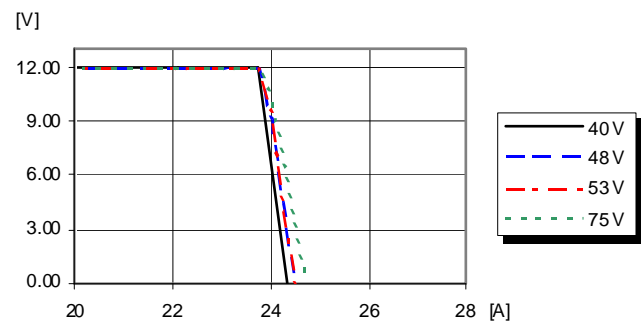
BMR 454 0000/001

Output Characteristics



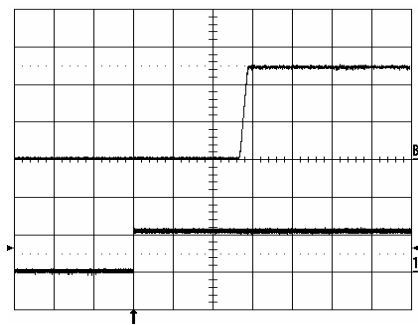
Output voltage vs. load current at $T_{ref} = +25^{\circ}\text{C}$

Current Limit Characteristics



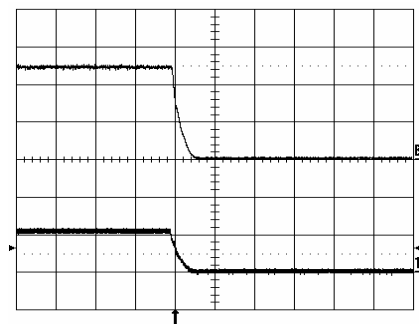
Output voltage vs. load current at $I_O > \max I_O$, $T_{ref} = +25^{\circ}\text{C}$

Start-up



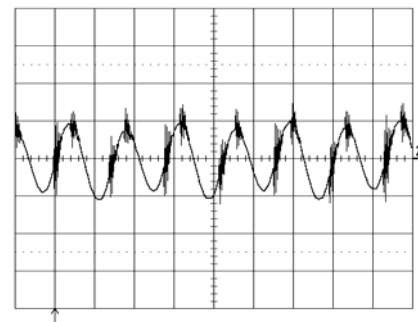
Start-up enabled by connecting V_I at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 20\text{ A}$ resistive load.
Top trace: output voltage (5 V/div.).
Bottom trace: input voltage (50 V/div.).
Time scale: (50 ms/div.).

Shut-down



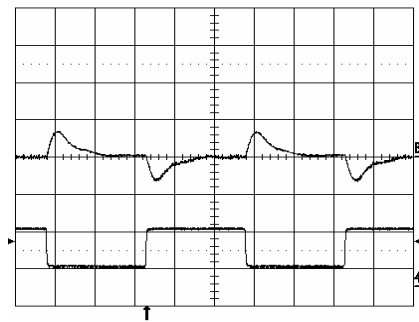
Shut-down enabled by disconnecting V_I at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 20\text{ A}$ resistive load.
Top trace: output voltage (5 V/div.).
Bottom trace: input voltage (50 V/div.).
Time scale: (0.5 ms/div.).

Output Ripple & Noise



Output voltage ripple at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 20\text{ A}$ resistive load.
Trace: output voltage (20 mV/div.).
Time scale: (2 μs /div.).

Output Load Transient Response



Output voltage response to load current step-
change (5 - 15 - 5 A) at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$, $C_o = 2.2\text{ mF}$
Top trace: output voltage (0.5 V/div.).
Bottom trace: output current (10 A/div.).
Time scale: (0.5 ms/div.).

BMR454 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 40 A / 240 W

EN/LZT 146 404 R5A July 2011

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12 V, 20 A / 240 W Electrical Specification
BMR 454 0004/005
 $T_{P1} = -40$ to $+90^{\circ}\text{C}$, $V_I = 36$ to 75 V, sense pins connected to output pins unless otherwise specified under Conditions.

 Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, $I_O = \text{max}$, unless otherwise specified under Conditions.

 Additional $C_{out} = 0.1$ mF, Configuration File: 190 10-CDA 102 1900/005 rev A

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage range		36		75	V
V_{loff}	Turn-off input voltage	Decreasing input voltage	32	33	34	V
V_{lon}	Turn-on input voltage	Increasing input voltage	34	35	36	V
C_I	Internal input capacitance			11		μF
P_O	Output power		0		240	W
η	Efficiency	50% of max I_O		94.8		%
		max I_O		94.9		
		50% of max I_O , $V_I = 48$ V		95.1		
		max I_O , $V_I = 48$ V		94.9		
P_d	Power Dissipation	max I_O		13.0	17.8	W
P_{li}	Input idling power	$I_O = 0$ A, $V_I = 53$ V		3.1		W
P_{RC}	Input standby power	$V_I = 53$ V (turned off with RC)		123		mW
f_s	Switching frequency	0-100% of max I_O see Note 2	171	180	189	kHz

V_{Oi}	Output voltage initial setting and accuracy	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, $I_O = 20$ A	11.88	12.0	12.12	V
V_O	Output adjust range	See operating information and Note 1	8.1		13.2	V
	Output voltage tolerance band	0-100 % of max I_O	11.76		12.24	V
	Line regulation	max I_O		22	80	mV
	Load regulation	$V_I = 53$ V, 0-100% of max I_O		15	57	mV
V_{tr}	Load transient voltage deviation	$V_I = 53$ V, Load step 25-75-25% of max I_O , $di/dt = 1$ A/ μs		± 0.3		V
t_{tr}	Load transient recovery time	see Note 3		250		μs
t_r	Ramp-up time (from 10-90% of V_{Oi})	10-100% of max I_O , $T_{P1} = 25^{\circ}\text{C}$, $V_I = 53$ V		8		ms
t_s	Start-up time (from V_I connection to 90% of V_{Oi})	see Note 4		140		ms
t_f	V_I shut-down fall time (from V_I off to 10% of V_O)	max I_O		0.4		ms
		$I_O = 0$ A		5		s
t_{RC}	RC start-up time	max I_O		55		ms
		max I_O		2.4		ms
		$I_O = 0$ A		5		s
I_O	Output current		0		20	A
I_{lim}	Current limit threshold	$V_O = 10.8$ V, $T_{P1} < \text{max } T_{ref}$	21	25	28	A
I_{sc}	Short circuit current	$T_{P1} = 25^{\circ}\text{C}$, see Note 5		4	5	A
C_{out}	Recommended Capacitive Load	$T_{P1} = 25^{\circ}\text{C}$, see Note 6	0.1	2.2	6	mF
V_{Oac}	Output ripple & noise	See ripple & noise section, max I_O		60	120	mVp-p
OVP	Over voltage protection	$T_{P1} = +25^{\circ}\text{C}$, $V_I = 53$ V, 10-100% of max I_O , see Note 7		15.6		V

Note 1: For output voltage below 11V, the BMR 454 0000/XXX is recommended for better efficiency and thermal performance.

Note 2: Frequency may be adjusted with PMBus communication. See Operating Information section

 Note 3: $C_{out} = 2.2$ mF used at load transient test.

Note 4: Start-up and Ramp-up time can be increased via PMBus, see Operation Information section.

Note 5: OCP in hiccup mode

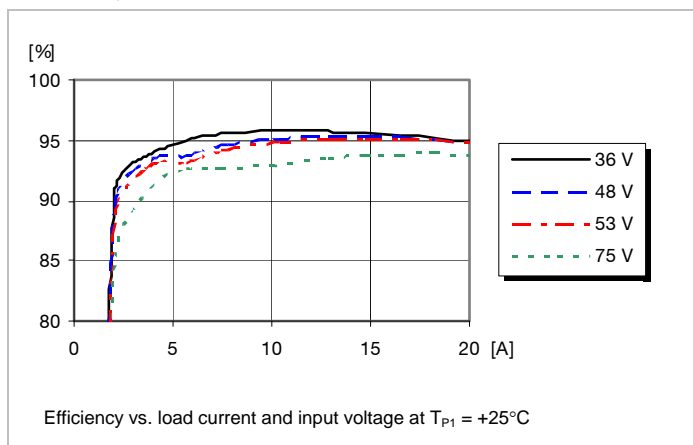
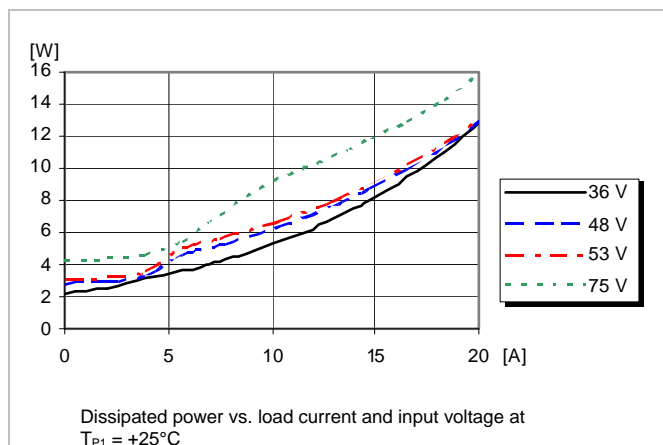
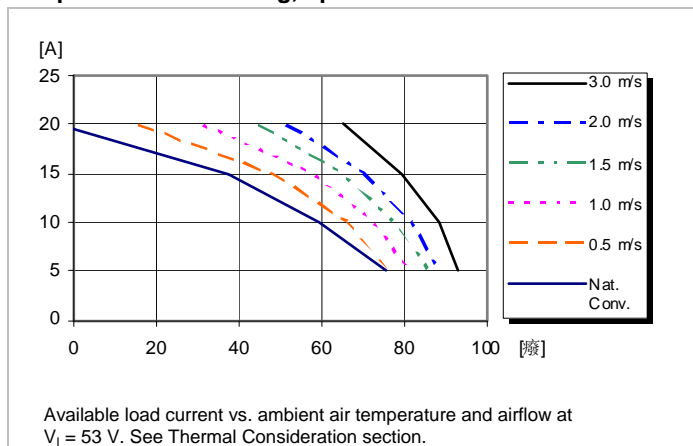
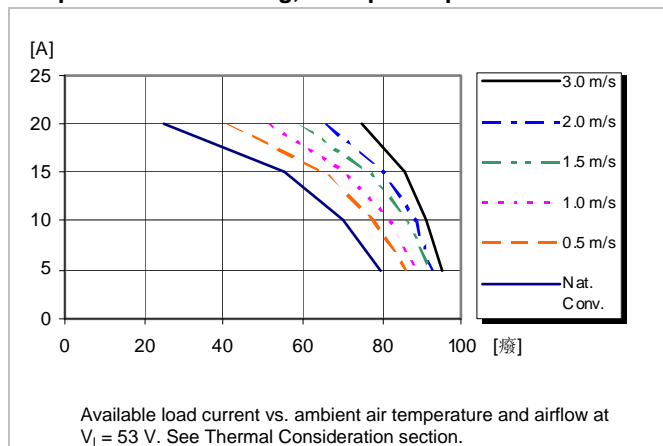
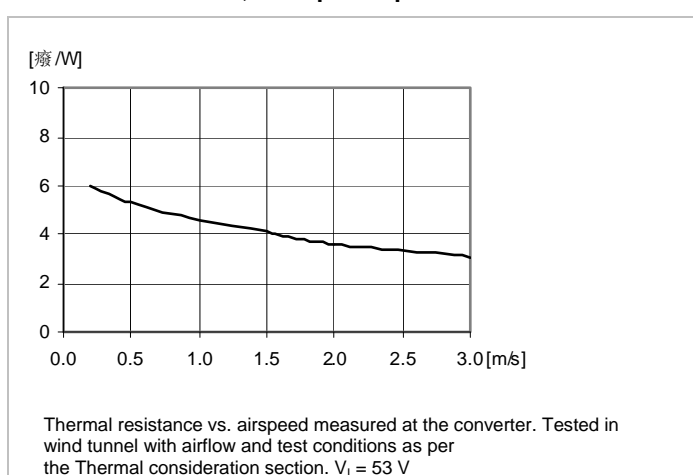
Note 6: Low ESR-value

Note 7: OVP-level can be adjusted via PMBus, see Operation Information section.

BMR454 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 40 A / 240 W

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12 V, 20 A / 240 W Typical Characteristics
BMR 454 0004/005
Efficiency

Power Dissipation

Output Current Derating, open frame

Output Current Derating, base plate option

Thermal Resistance, base plate option


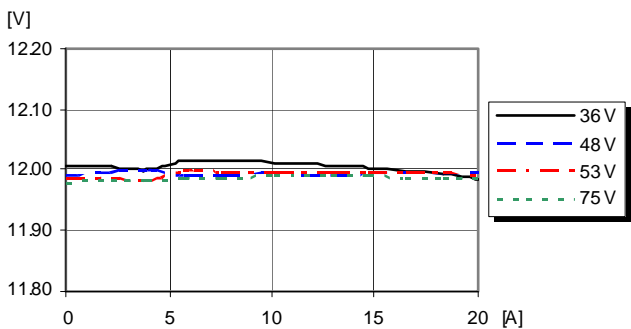
BMR454 series Fully regulated Intermediate Bus Converters
Input 36-75 V, Output up to 40 A / 240 W

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12 V, 20 A / 240 W Electrical Specification

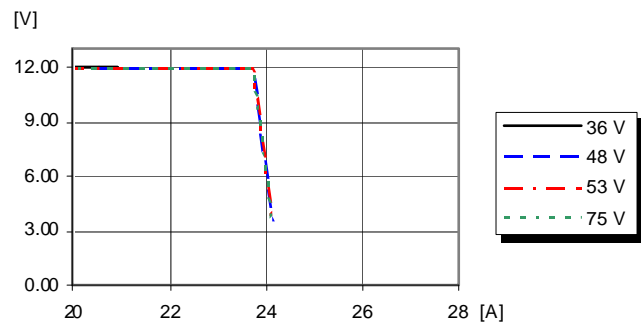
BMR 454 0004/005

Output Characteristics



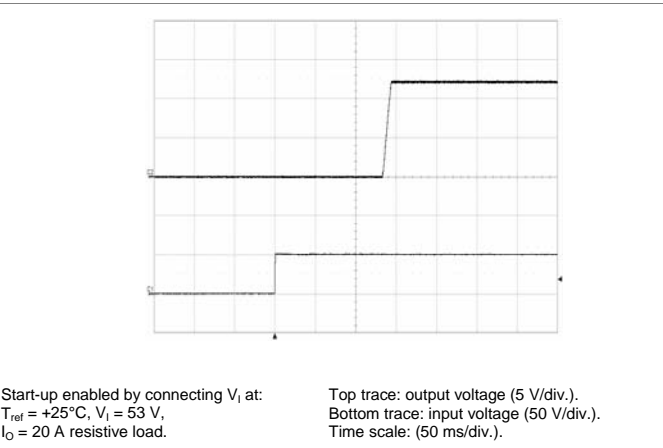
Output voltage vs. load current at $T_{ref} = +25^{\circ}\text{C}$

Current Limit Characteristics



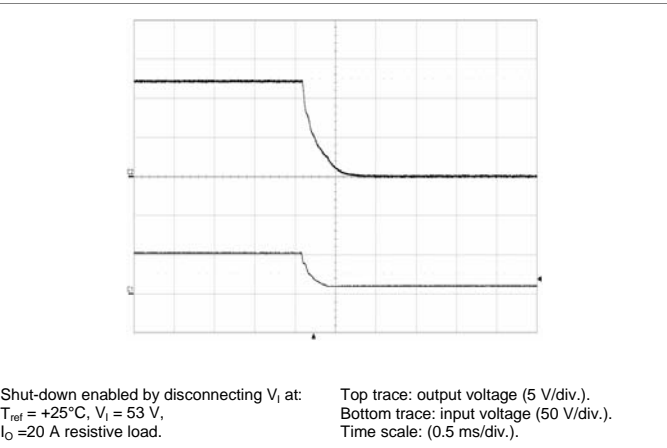
Output voltage vs. load current at $I_O > \max I_O$, $T_{ref} = +25^{\circ}\text{C}$

Start-up



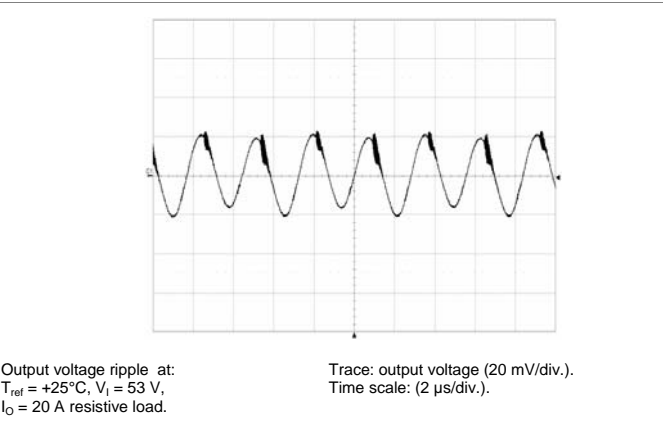
Start-up enabled by connecting V_I at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 20\text{ A}$ resistive load.
Top trace: output voltage (5 V/div.).
Bottom trace: input voltage (50 V/div.).
Time scale: (50 ms/div.).

Shut-down



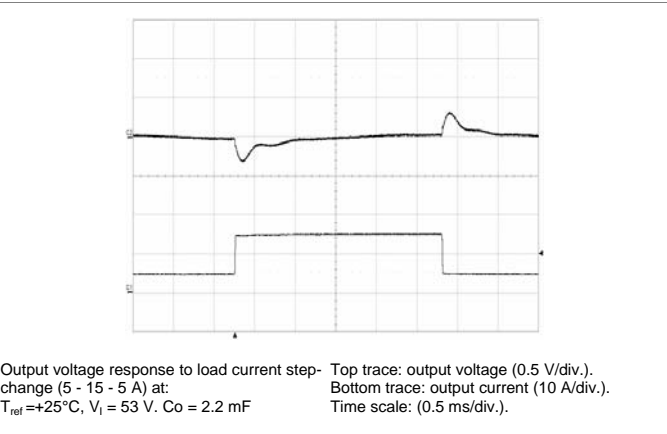
Shut-down enabled by disconnecting V_I at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 20\text{ A}$ resistive load.
Top trace: output voltage (5 V/div.).
Bottom trace: input voltage (50 V/div.).
Time scale: (0.5 ms/div.).

Output Ripple & Noise



Output voltage ripple at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$,
 $I_O = 20\text{ A}$ resistive load.
Trace: output voltage (20 mV/div.).
Time scale: (2 μs/div.).

Output Load Transient Response



Output voltage response to load current step-
change (5 - 15 - 5 A) at:
 $T_{ref} = +25^{\circ}\text{C}$, $V_I = 53\text{ V}$, $C_o = 2.2\text{ mF}$
Top trace: output voltage (0.5 V/div.).
Bottom trace: output current (10 A/div.).
Time scale: (0.5 ms/div.).

BMR454 series Fully regulated Intermediate Bus Converters
Input 36-75 V, Output up to 40 A / 240 W

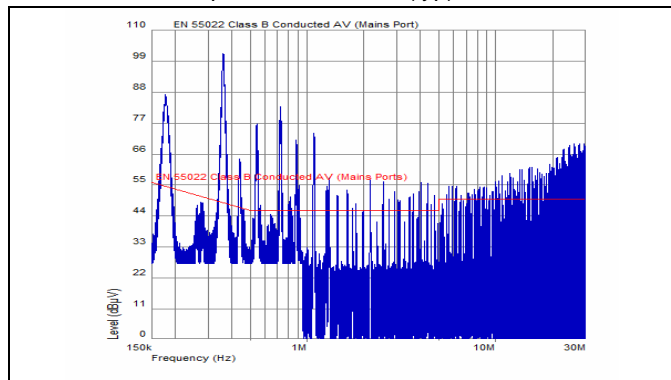
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EMC Specification

Conducted EMI measured according to EN55022, CISPR 22 and FCC part 15J (see test set-up). See Design Note 009 for further information. The fundamental switching frequency is 180 kHz for BMR 454 at $V_I = 53$ V, max I_O .

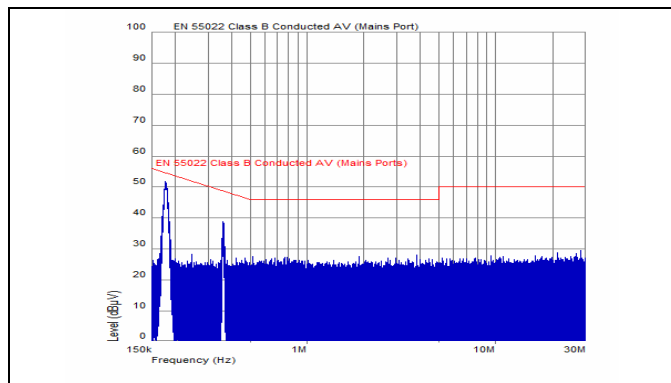
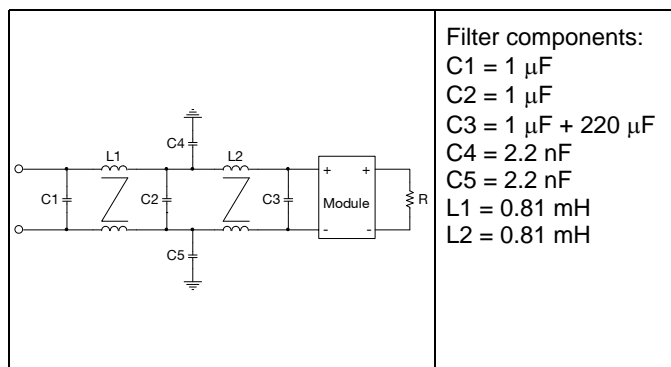
Conducted EMI Input terminal value (typ)



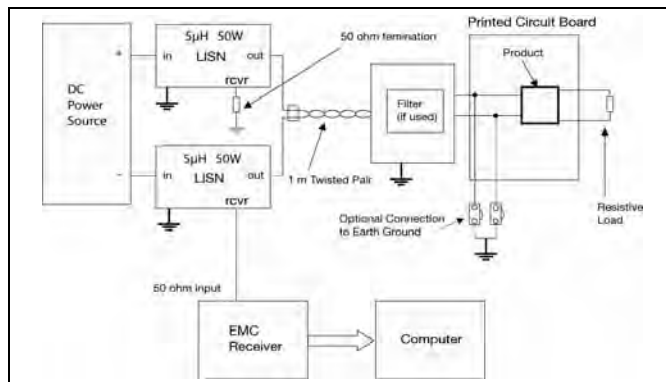
EMI without filter

External filter (class B)

Required external input filter in order to meet class B in EN 55022, CISPR 22 and FCC part 15J.



EMI with filter



Test set-up

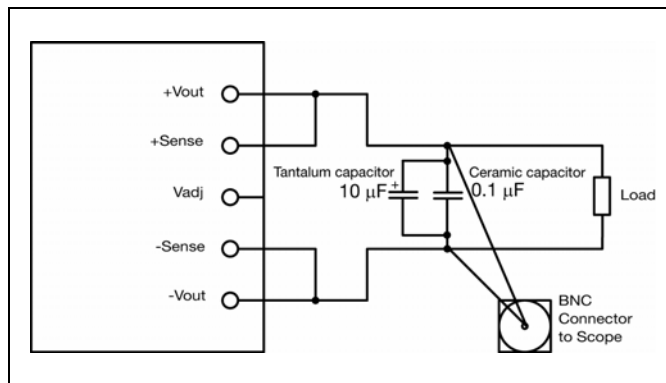
Layout recommendations

The radiated EMI performance of the product will depend on the PWB layout and ground layer design. It is also important to consider the stand-off of the product. If a ground layer is used, it should be connected to one of the output terminals and the equipment ground or chassis.

A ground layer will increase the stray capacitance in the PWB and improve the high frequency EMC performance.

Output ripple and noise

Output ripple and noise measured according to figure below. See Design Note 022 for detailed information.



Output ripple and noise test setup

BMR454 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 40 A / 240 W

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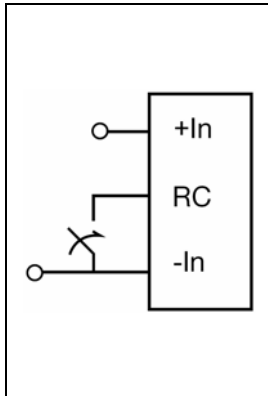
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Operating information
Input Voltage

The input voltage range 36 to 75 Vdc meets the requirements of the European Telecom Standard ETS 300 132-2 for normal input voltage range in -48 and -60 Vdc systems, -40.5 to -57.0 V and -50.0 to -72 V respectively. At input voltages exceeding 75 V, the power loss will be higher than at normal input voltage and T_{P1} must be limited to absolute max +125°C. The absolute maximum continuous input voltage is 80 Vdc.

Turn-off Input Voltage

The product monitors the input voltage and will turn on and turn off at predetermined levels. The turn on and turn off level and the hysteresis in between can be configured via the PMBus. The default hysteresis between turn on and turn off input voltage is set to 2 V.

Remote Control (RC)


The products are fitted with a configurable remote control function on the primary and secondary side. The primary remote control is referenced to the primary negative input connection (-In). The RC function allows the converter to be turned on/off by an external device like a semiconductor or mechanical switch. The RC pin has an internal pull up resistor. The remote control functions can also be configured using the PMBus.

The device should be capable of sinking 0.7 mA. When the RC pin is left open, the voltage generated on the RC pin is max 6 V. The standard product is provided with "negative logic" remote control and will be off until the RC pin is connected to the -In. To turn on the product the voltage between RC pin and -In should be less than 1 V. To turn off the product the RC pin should be left open. In situations where it is desired to have the product to power up automatically without the need for control signals or a switch, the RC pin can be wired directly to -In. The logic option for the primary remote control is configured using the PMBus.

Remote Control (secondary side)

The CTRL CS pin can be configured as remote control via the PMBus interface. In the default configuration the CTRL CS pin is disabled and the output has an internal pull-up to 3.3 V. The CTRL CS pin can be left open when not used. The logic options for the secondary remote control can be positive or negative logic.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that

the input source has low characteristic impedance. Minimum recommended external input capacitance is 100 uF. The performance in some applications can be enhanced by addition of external capacitance as described under External Decoupling Capacitors.

External Decoupling Capacitors

When powering loads with significant dynamic current requirements, the voltage regulation at the point of load can be improved by addition of decoupling capacitors at the load. The recommended minimum capacitance on the output is 100 uF. The most effective technique is to locate low ESR ceramic and electrolytic capacitors as close to the load as possible, using several parallel capacitors to lower the effective ESR. The ceramic capacitors will handle high-frequency dynamic load changes while the electrolytic capacitors are used to handle low frequency dynamic load changes. Ceramic capacitors will also reduce any high frequency noise across the load.

External decoupling capacitors will become part of the product's control loop. The control loop is optimized for a wide range of external capacitance and the maximum recommended value that could be used without any additional analysis is found in the Electrical specification. The ESR of the capacitors is a very important parameter. Stable operation is guaranteed with a verified ESR value of >10 mΩ across the output connections. For further information please contact your local Ericsson Power Modules representative.

Parallel Operation

The products can be paralleled for redundancy if external oring diodes are used in series with the output.

PMBus configuration and support

The products provide a PMBus digital interface that enables the user to configure many aspects of the device operation as well as monitor the input and output parameters. Please contact your local Ericsson Power Modules representative for appropriate SW tools to down-load new configurations.

Output Voltage Adjust using PMBus

The output voltage of the product can be reconfigured using the PMBus interface. Both BMR 454 0000/XXX and BMR 454 0004/005 can be adjusted from 8.1 V to 13.2 V. However, if output voltages above 11 V are desired at full load and at input below 40 V, the BMR4540004/005 should be used. When output voltages below 11V are desired or the limited input range (40-75 V) is acceptable, the BMR4540000/XXX is recommended for better efficiency and thermal performance. The BMR 454 0002/XXX can be adjusted from 3.0 V to 6.7 V at input voltages from 36 V to 75 V.

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Margin Up/Down Controls

These controls allow the output voltage to be momentarily adjusted, either up or down, by a nominal 10%. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. The margin up and down levels of the product can be re-configured using the PMBus interface.

Soft-start Power Up

The soft-start control introduces a time-delay (default setting 40 ms) before allowing the output voltage to rise. The default rise time of the ramp up is 10 ms. Power-up is hence completed within 50 ms in default configuration using remote control. When starting by applying input voltage the control circuit boot-up time adds an additional 100 ms delay. The soft-start power up of the product can be reconfigured using the PMBus interface.

Remote Sense

The products have remote sense that can be used to compensate for voltage drops between the output and the point of load. The sense traces should be located close to the PCB ground layer to reduce noise susceptibility. The remote sense circuitry will compensate for up to 10% voltage drop between +Out pin and the point of load (+Sense). The -Sense pin should be always connected to -Out. When activating remote sense, connect the +Sense pin to the +Input of the load. If the remote sense is not needed +Sense pin should be connected to +Out of the BMR454 unit. To be able to use remote sense the converter must be equipped with a digital connector.

Temperature Protection (OTP, UTP)

The products are protected from thermal overload by an internal temperature shutdown protection. When T_{P1} as defined in thermal consideration section is exceeded the product will shut down. The product will make continuous attempts to start up (non-latching mode) and resume normal operation automatically when the temperature has dropped below the temperature threshold, the hysteresis is defined in general electrical specification. The OTP and hysteresis of the product can be re-configured using the PMBus interface. The product has also an under temperature protection. The OTP and UTP fault limit and fault response can be configured via the PMBus. Note: using the fault response "continue without interruption" may cause permanent damage of the product.

Over Voltage Protection (OVP)

The product has output over voltage protection that will shut down the converter in over voltage conditions (latching mode). The OVP fault level and fault response can be re-configured using the PMBus interface.

Over Current Protection (OCP)

The product includes current limiting circuitry for protection at

continuous overload. The product will enter hic-up mode if the maximum output current is exceeded and the output voltage is below $0.3 \times V_{out}$. The load distribution should be designed for the maximum output short circuit current specified. The OCP level and fault response can be re-configured using the PMBus interface. The default OCP configuration is set to hic-up mode for the over current protection.

Input Over/Under voltage protection

The input of the product can be protected against high input voltage and low input voltage. The over- and under-voltage fault level and fault response can be configured via the PMBus interface.

Pre-bias Start-up

The product has a Pre-bias start up functionality and will not sink current during start up if a pre-bias source is present at the output terminals.

Synchronization

When the PG SYNC pin is configured as an input (SYNC IN) the device will automatically check for a clock signal on the PG SYNC pin each time the module is enabled by RC or via PMBus. The incoming clock signal must be 150, 200 or 250 kHz and must be stable when the module is enabled. Note that PG SYNC pin is by default configured as Power Good output but may be reconfigured to SYNC IN via the PMBus interface.

Power Good

The PG SYNC pin is by default configured as Power Good output. The power good signal (TTL level) indicates proper operation of the product and can also be used as an error flag indicator. The Power Good signal is by default configured as active low and can be re-configured via the PMBus interface.

Tracking and External reference

The PG SYNC pin can be configured as an input for voltage tracking or an external analogue reference. The PG SYNC pin is configured via the PMBus interface and has default setting Power Good.

Switching frequency adjust using PMBus

The switching frequency is set to 180 kHz as default but this can be reconfigured via the PMBus interface. The product is optimized at this frequency but can run at lower and higher frequency, (150 kHz – 250 kHz). The electrical performance can be affected if the switching frequency is changed.

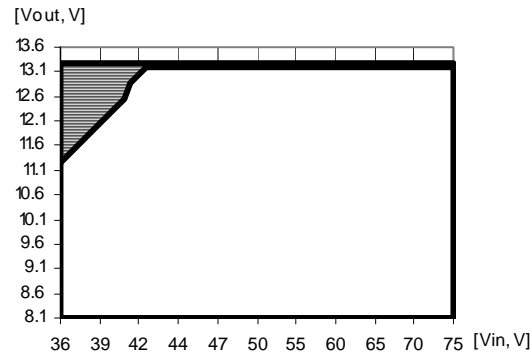
Input Transient

The BMR454 products have limited ability to react on sudden input voltage changes. As an example the 12 V module BMR454xxxx/001 can have an output voltage deviation of 5 V when a 20V input step is applied (40 V to 60 V). This is tested with a slew rate of 0.1 V/us on the input voltage change and minimum output capacitance 100 uF. Increasing the output capacitance will improve the result.

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Input 36-75 V, Output up to 40 A / 240 W

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BMR4540000/001 Output voltage regulation



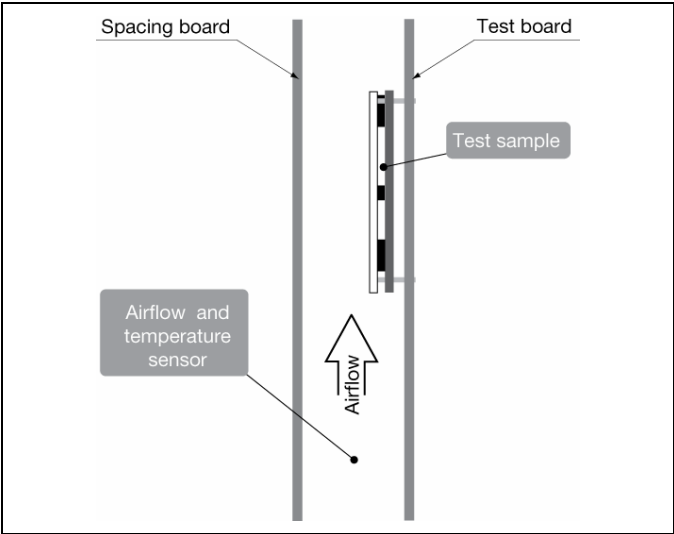
Output voltage regulation vs input voltage at: TP1 = +25°C, IO = 20 A resistive load, The output voltage will be fully regulated for all operating combinations within the white area in the plot above. Operation outside of this area is not recommended for normal use. (Note 20 A is maximum load current at start-up)

Thermal Consideration

General

The products are designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation.
For products mounted on a PWB without a heat sink attached, cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependant on the airflow across the product. Increased airflow enhances the cooling of the product. The Output Current Derating graph found in the Output section for each model provides the available output current vs. ambient air temperature and air velocity at V_I = 53 V.

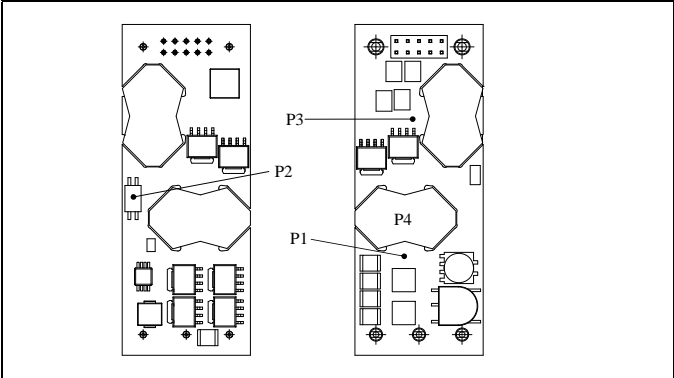
The product is tested on a 254 x 254 mm, 35 µm (1 oz), 8-layer test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm.



Definition of product operating temperature

The product operating temperatures is used to monitor the temperature of the product, and proper thermal conditions can be verified by measuring the temperature at positions P1, P2 and P3. The temperature at these positions (T_{P1}, T_{P2} and T_{P3}) should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above maximum T_{P1}, measured at the reference point P1 are not allowed and may cause permanent damage.

Position	Description	Max Temperature
P1	PCB (Reference point)	T _{P1} ≦125° C
P2	Opto-coupler	T _{P2} ≦105° C
P3	PCB (Output inductor)	T _{P3} ≦125° C
P4	Transformer core	T _{P4} ≦125° C



Top view Bottom view
(Best airflow direction right to left.)

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Input 36-75 V, Output up to 40 A / 240 W

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Ambient Temperature Calculation

For products with base plate the maximum allowed ambient temperature can be calculated by using the thermal resistance.

- 1. The power loss is calculated by using the formula $((1/\eta) - 1) \times \text{output power} = \text{power losses (Pd)}$.
 η = efficiency of product. E.g. 95% = 0.95
- 2. Find the thermal resistance (Rth) in the Thermal Resistance graph found in the Output section for each model. **Note that the thermal resistance can be significantly reduced if a heat sink is mounted on the top of the base plate.**

Calculate the temperature increase (ΔT).
 $\Delta T = R_{th} \times P_d$

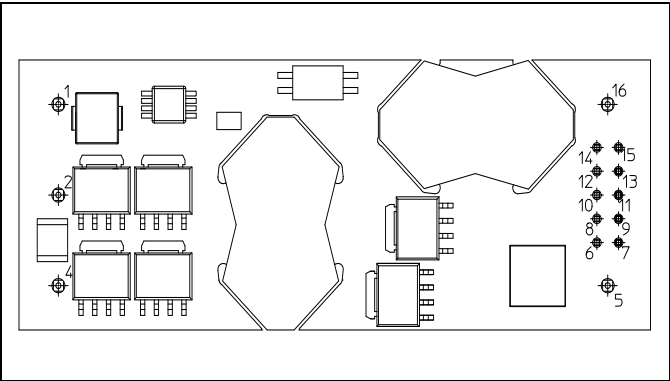
- 3. Max allowed ambient temperature is:
 $\text{Max } T_{P1} - \Delta T$.

E.g. BMR 454 0100/001 at 1m/s:

- 1. $((\frac{1}{0.94}) - 1) \times 240 \text{ W} = 15.3 \text{ W}$
- 2. $15.3 \text{ W} \times 4.1^\circ\text{C/W} = 63^\circ\text{C}$
- 3. $125^\circ\text{C} - 63^\circ\text{C} = \text{max ambient temperature is } 62^\circ\text{C}$

The actual temperature will be dependent on several factors such as the PCB size, number of layers and direction of airflow.

Connections (Top view)



Pin	Designation	Function
1	+In	Positive Input
2	RC	Remote Control
4	-In	Negative Input
5	-Out	Negative Output
6	S+	Positive Remote Sense
7	S-	Negative Remote Sense
8	SA0	Address pin 0
9	SA1	Address pin 1
10	SCL	PMBus Clock
11	SDA	PMBus Data
12	PG SYNC	Configurable I/O pin: Power Good output, SYNC-, tracking-, or ext ref-input
13	DGND	PMBus ground
14	SALERT	PMBus alert signal
15	CTRL CS	PMBus remote control
16	+Out	Positive Output

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PMBus Communications

The products provide a PMBus digital interface that enables the user to configure many aspects of the device operation as well as monitor the input and output parameters. The products can be used with any standard two-wire I²C or SMBus host device. In addition, the device is compatible with PMBus version 1.1 and includes an SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring.

Monitoring via PMBus

A system controller can monitor a wide variety of different parameters through the PMBus interface. The controller can monitor for fault condition by monitoring the SALERT pin, which will be asserted when any number of pre-configured fault or warning conditions occur. The system controller can also continuously monitor for any number of power conversion parameters including but not limited to the following:

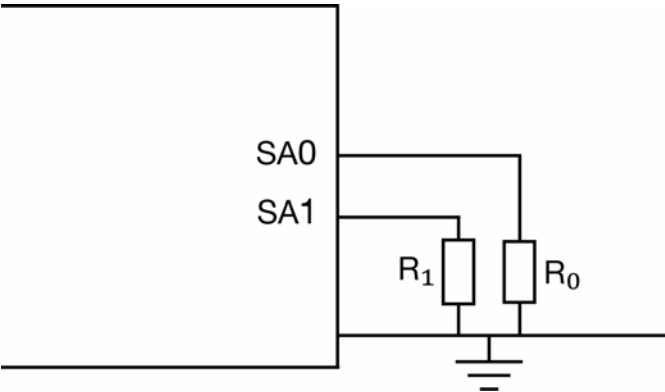
- Input voltage
- Output voltage
- Output current
- Internal junction temperature
- Switching frequency
- Duty cycle

Evaluation software

A Configuration Monitoring and Management (CMM) evaluation software, is available for the products. For more information please contact your local Ericsson Power Modules sales representative.

Addressing

The figure and table below show recommended resistor values with min and max voltage range for hard-wiring PMBus addresses (series E96, 1% tolerance resistors suggested):



SA0/SA1	R ₁ /R ₀ [kΩ]	Min voltage[V]	Max voltage[V]
0	24.9	0.261	0.438
1	49.9	0.524	0.679
2	75	0.749	0.871
3	100	0.926	1.024
4	124	1.065	1.146
5	150	1.187	1.256
6	174	1.285	1.345
7	200	1.371	1.428

The SA0 and SA1 pins can be configured with a resistor to GND according to the following equation.

PMBus Address = 8 x (SA0value) + (SA1 value)

If any one of those voltage applied to ADC0 and ADC1 is out of the range from the table above, PMBus address 127 is assigned. If the calculated PMBus address is 0 or 12, PMBus address 127 is assigned instead. PMBus address 11 is not to be used. The user shall also be aware of further limitations of the addresses as stated in the PMBus Specification.

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PMBus Commands

The DC/DC converter is PMBUS compliant. The following table lists the implemented PMBus commands. For more detailed information see PMBus Power System Management Protocol Specification; Part I – General Requirements, Transport and Electrical Interface and PMBus Power System Management Protocol; Part II – Command Language.

Designation	Cmd	Impl
Standard PMBus Commands		
Control Commands		
PAGE	00h	No
OPERATION	01h	Yes
ON_OFF_CONFIG	02h	Yes
WRITE_PROTECT	10h	Yes
Output Commands		
VOUT_MODE	20h	Yes
VOUT_COMMAND	21h	Yes
VOUT_TRIM	22h	Yes
VOUT_GAIN	23h	Yes ^{note1}
VOUT_MAX	24h	Yes
VOUT_MARGIN_HIGH	25h	Yes
VOUT_MARGIN_LOW	26h	Yes
VOUT_TRANSITION_RATE	27h	Yes
VOUT_DROOP	28h	No
VOUT_SCALE_LOOP	29h	Yes ^{note1}
VOUT_SCALE_MONITOR	2Ah	Yes ^{note1}
COEFFICIENTS	30h	No
POUT_MAX	31h	No
MAX_DUTY	32h	Yes
FREQUENCY_SWITCH	33h	Yes
VIN_ON	35h	Yes
VIN_OFF	36h	Yes
IOUT_CAL_GAIN	38h	Yes ^{note1}
IOUT_CAL_OFFSET	39h	Yes ^{note1}
Fault Limit Commands		
POWER_GOOD_ON	5Eh	Yes
POWER_GOOD_OFF	5Fh	Yes
VOUT_OV_FAULT_LIMIT	40h	Yes
VOUT_UV_FAULT_LIMIT	44h	Yes
IOUT_OC_FAULT_LIMIT	46h	Yes
IOUT_OC_LV_FAULT_LIMIT	48h	Yes
IOUT_UC_FAULT_LIMIT	4Bh	No
OT_FAULT_LIMIT	4Fh	Yes

Designation	Cmd	Impl
OT_WARN_LIMIT	51h	Yes
UT_WARN_LIMIT	52h	Yes
UT_FAULT_LIMIT	53h	Yes
VIN_OV_FAULT_LIMIT	55h	Yes
VIN_OV_WARN_LIMIT	57h	Yes
VIN_UV_WARN_LIMIT	58h	Yes
VIN_UV_FAULT_LIMIT	59h	Yes
VOUT_OV_WARN_LIMIT	42h	Yes
VOUT_UV_WARN_LIMIT	43h	Yes
IOUT_OC_WARN_LIMIT	4Ah	Yes
IIN_OC_FAULT_LIMIT	5Bh	No
IIN_OC_WARN_LIMIT	5Dh	No
Fault Response Commands		
VOUT_OV_FAULT_RESPONSE	41h	Yes
VOUT_UV_FAULT_RESPONSE	45h	Yes
OT_FAULT_RESPONSE	50h	Yes
UT_FAULT_RESPONSE	54h	Yes
VIN_OV_FAULT_RESPONSE	56h	Yes
VIN_UV_FAULT_RESPONSE	5Ah	Yes
IOUT_OC_FAULT_RESPONSE	47h	Yes
IOUT_UC_FAULT_RESPONSE	4Ch	No
IIN_OC_FAULT_RESPONSE	5Ch	No
Time setting Commands		
TON_DELAY	60h	Yes
TON_RISE	61h	Yes
TON_MAX_FAULT_LIMIT	62h	Yes
TON_MAX_FAULT_RESPONSE	63h	Yes
TOFF_DELAY	64h	Yes
TOFF_FALL	65h	Yes
TOFF_MAX_WARN_LIMIT	66h	Yes
Status Commands (Read Only)		
CLEAR_FAULTS	03h	Yes
STATUS_BYTES	78h	Yes
STATUS_WORD	79h	Yes
STATUS_VOUT	7Ah	Yes
STATUS_IOUT	7Bh	Yes
STATUS_INPUT	7Ch	Yes
STATUS_TEMPERATURE	7Dh	Yes
STATUS_CML	7Eh	Yes
STATUS_OTHER	7Fh	Yes
Monitor Commands (Read Only)		
READ_VIN	88h	Yes

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Designation	Cmd	Impl
READ_VOUT	8Bh	Yes
READ_IOUT	8Ch	Yes
READ_TEMPERATURE_1	8Dh	Yes
READ_TEMPERATURE_2	8Eh	Yes
READ_FAN_SPEED_1	90h	No
READ_DUTY_CYCLE	94h	Yes
READ_FREQUENCY	95h	Yes
READ_POUT	96h	No
READ_PIN	97h	No
Identification Commands (Read Only)		
PMBUS_REVISION	98h	Yes
MFR_ID	99h	Yes ^{note1}
MFR_MODEL	9Ah	Yes ^{note1}
MFR_REVISION	9Bh	Yes ^{note1}
MFR_LOCATION	9Ch	Yes ^{note1}
MFR_DATE	9Dh	Yes ^{note1}
MFR_SERIAL	9Eh	Yes ^{note1}
Group Commands		
INTERLEAVE	37h	No
Supervisory Commands		
STORE_DEFAULT_ALL	11h	Yes
RESTORE_DEFAULT_ALL	12h	Yes
STORE_USER_ALL	15h	No
RESTORE_USER_ALL	16h	No
BMR 453/454 Specific Commands		
MFR_POWER_GOOD_POLARITY	D0h	Yes
MFR_VOUT_UPPER_RESISTOR	D2h	Yes ^{note1}
MFR_VIN_SCALE_MONITOR	D3h	Yes ^{note1}
MFR_CLA_TABLE_NUM_ROW	D4h	Yes
MFR_CLA_ROW_COEFFICIENTS	D5h	Yes
MFR_STORE_CLA_TABLE	D6h	Yes
MFR_ACTIVE_COEFF_CLA_TABLE	D8h	Yes
MFR_SET_ROM_MODE	D9h	Yes ^{note1}
MFR_SELECT_TEMP_SENSOR	DCh	Yes
MFR_VIN_OFFSET	DDh	Yes ^{note1}
MFR_REMOTE_TEMP_CAL	E2h	Yes
MFR_REMOTE_CONTROL	E3h	Yes
MFR_DEAD_BAND_MODE	E4h	Yes ^{note1}
MFR_DEAD_BAND_DELAY	E5h	Yes ^{note1}
MFR_TEMP_COEFF	E7h	Yes ^{note1}
MFR_VOUT_ANALOG_SCALE	E8h	Yes
MFR_READ_VOUT_ANALOG_REF	E9h	Yes

Designation	Cmd	Impl
MFR_DEBUG_BUFF	F0h	Yes
MFR_SETUP_PASSWORD	F1h	Yes
MFR_DISABLE_SECURITY	F2h	Yes
MFR_DEAD_BAND_IOUT_THRESHOLD	F3h	Yes ^{note1}
MFR_SECURITY_BIT_MASK	F4h	Yes
MFR_PRIMARY_TURN	F5h	Yes ^{note1}
MFR_SECONDARY_TURN	F6h	Yes ^{note1}
MFR_SET_DPWM_POLARITY	F7h	Yes ^{note1}
MFR_ILIM_SOFTSTART	F8h	Yes
MFR_MULTI_PIN_CONFIG	F9h	Yes
MFR_DEAD_BAND_VIN_THRESHOLD	FAh	Yes ^{note1}
MFR_DEAD_BAND_VIN_IOUT_HYS	FBh	Yes ^{note1}
MFR_FIRMWARE_VERSION	FCh	Yes ^{note1}
MFR_MESSAGE_CODE_DEVICE_ID	FDh	Yes ^{note1}

Notes:

Cmd is short for Command.
 Impl is short for Implemented.

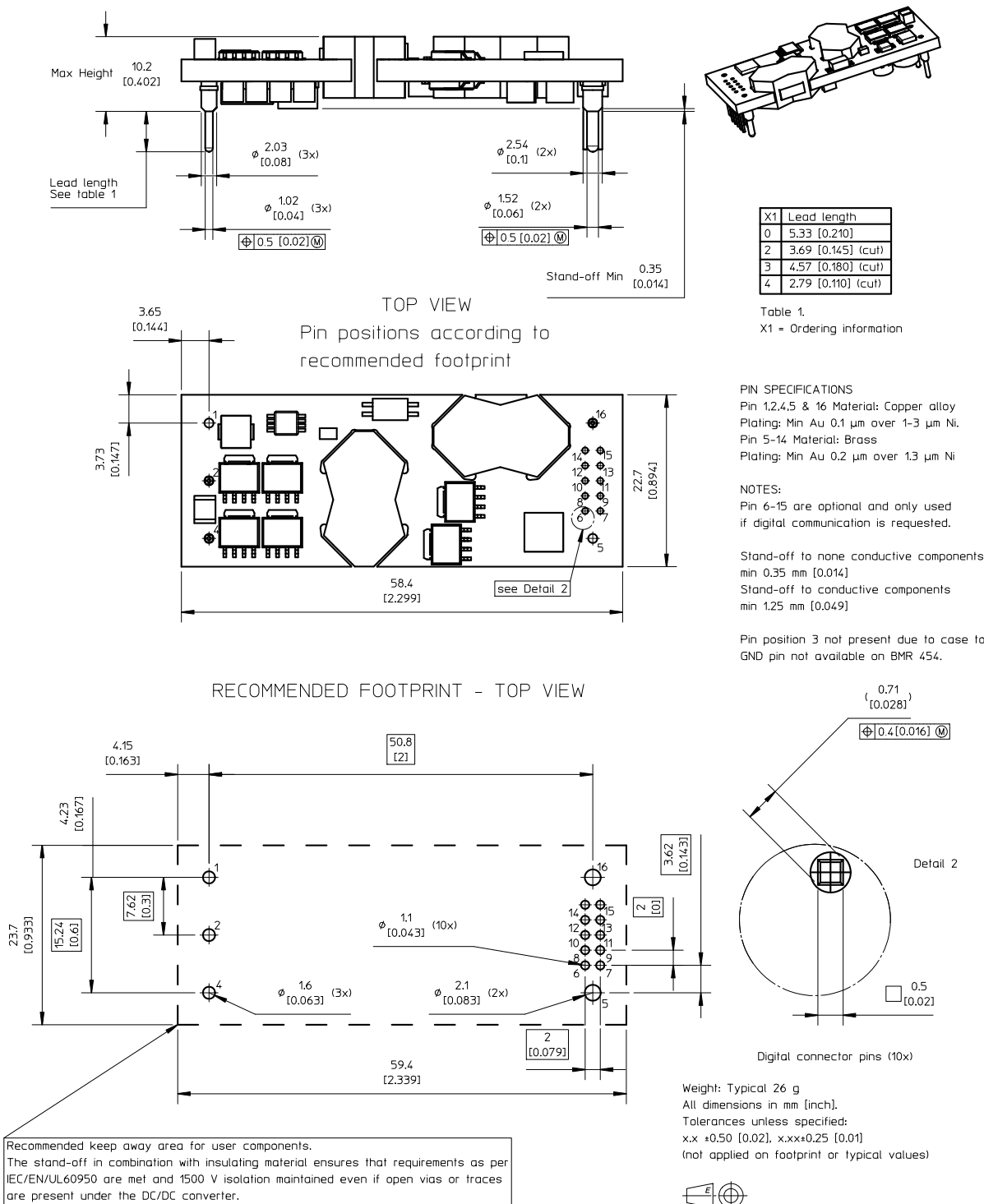
Note1:

the content is protected for being overwritten to secure normal operation

BMR454 series Fully regulated Intermediate Bus Converters
 Input 36-75 V, Output up to 40 A / 240 W

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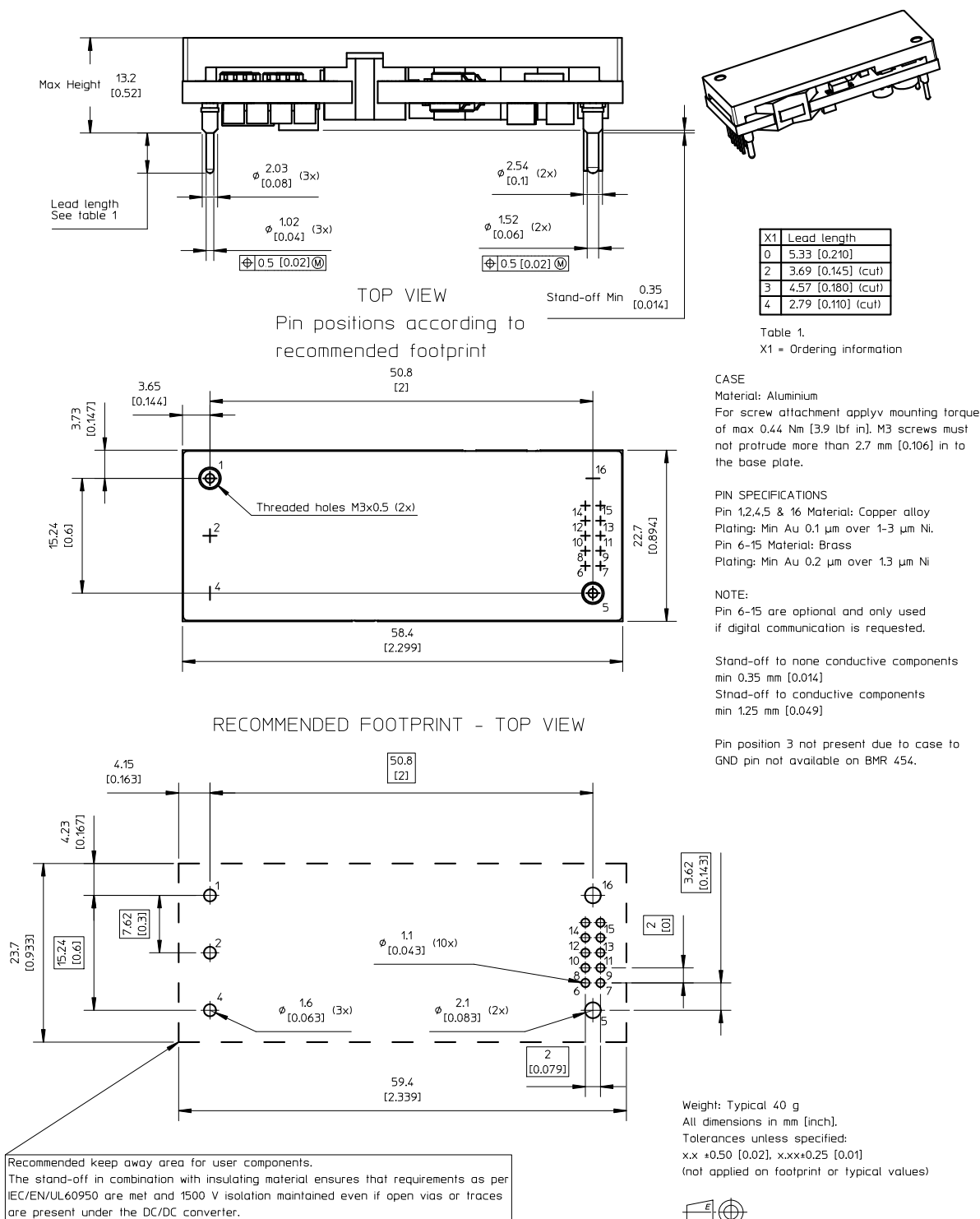
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Mechanical Information - Hole Mount, Open Frame Version


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 Input 36-75 V, Output up to 40 A / 240 W

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Mechanical Information- Hole Mount, Base Plate Version


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Soldering Information – Hole Mounting

The hole mounted product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds.

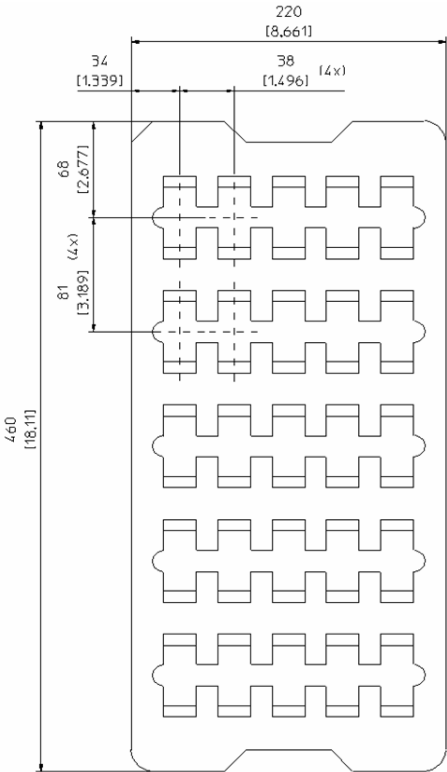
A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

Delivery package information

The products are delivered in antistatic trays.

Tray specifications	
Material	PE foam, dissipative
Surface resistance	10 ⁵ to 10 ¹² ohms/square
Tray capacity	25 converters/tray
Box capacity	75 converters
Weight	Product - Open frame 790 g full tray, 140 g empty tray Product – Base plate option 1265 g full tray, 140 g empty tray



BMR454 series Fully regulated Intermediate Bus Converters Input 36-75 V, Output up to 40 A / 240 W	EN/LZT 146 404 R5A July 2011
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Product Qualification Specification

Characteristics			
External visual inspection	IPC-A-610		
Change of temperature (Temperature cycling)	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 100°C 1000 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature T _A Duration	-45°C 72 h
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85 % RH 1000 hours
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 h
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Glycol ether Isopropyl alcohol	55°C 35°C 35°C
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Moisture reflow sensitivity ¹	J-STD-020C	Level 1 (SnPb-eutectic) Level 3 (Pb Free)	225°C 260°C
Operational life test	MIL-STD-202G, method 108A	Duration	1000 h
Resistance to soldering heat ²	IEC 60068-2-20 Tb, method 1A	Solder temperature Duration	270°C 10-13 s
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability	IEC 60068-2-58 test Td ¹	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	150°C dry bake 16 h 215°C 235°C
	IEC 60068-2-20 test Ta ²	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	Steam ageing 235°C 245°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g ² /Hz 10 min in each direction

Notes

¹ Only for products intended for reflow soldering (surface mount products)

² Only for products intended for wave soldering (plated through hole products)

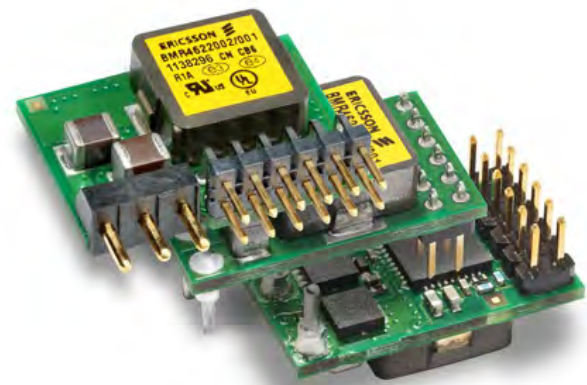
BMR 462 series POL Regulators Input 4.5-14 V, Output up to 12 A / 60 W	EN/LZT 146 436 R2A September 2011
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Key Features

- Small package
Laydown: 21.0 x 12.7 x 8.2 mm (0.827 x 0.5 x 0.323 in)
SIP: 20.8 x 7.6 x 15.6 mm (0.82 x 0.3 x 0.612 in)
- 0.6 V - 5.0 V output voltage range
- High efficiency, typ. 97.1% at 5Vin, 3.3Vout half load
- Configuration and Monitoring via PMBus
- Synchronization & phase spreading
- Voltage Tracking & Voltage margining
- MTBF 22 Mh

General Characteristics

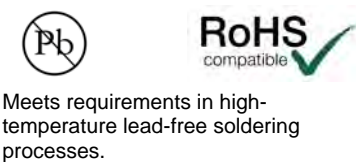
- Fully regulated
- For narrow board pitch applications (15 mm/0.6 in)
- Non-Linear Response for reduction of decoupling cap.
- Input under voltage shutdown
- Over temperature protection
- Output short-circuit & Output over voltage protection
- Remote control & Power Good
- Voltage setting via pin-strap or PMBus
- Advanced Configurable via Graphical Used Interface
- ISO 9001/14001 certified supplier
- Highly automated manufacturing ensures quality



Safety Approvals



Design for Environment



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Technical Specification

BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

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Ordering Information

Product program	Output
BMR 462	0.6-5.0 V, 20 A / 60 W

Product number and Packaging

BMR 462 n ₁ n ₂ n ₃ n ₄ /n ₅ n ₆ n ₇ n ₈									
Options	n ₁	n ₂	n ₃	n ₄	/	n ₅	n ₆	n ₇	n ₈
Mounting	o				/				
Mechanical		o			/				
Digital interface			o	o	/				
Configuration file					/	o	o	o	
Packaging					/				o

Options	Description
n ₁	0 Through hole mount version (TH) 1 Surface mount version (SMD) 2 Single in line (SIP)
n ₂	0 Open frame
n ₃ n ₄	02 PMBus and analog pin strap
n ₅ n ₆ n ₇	001 Standard configuration
n ₈	B Antistatic tray of 100 products (SIP only) C Antistatic tape & reel of 200 products (Sample delivery available in lower quantities. Not for SIP)

Example: Product number BMR 462 0002/001C equals a through-hole mounted, open frame, PMBus and analog pin strap, standard configuration variant.

General Information

Reliability

The failure rate (λ) and mean time between failures (MTBF = $1/\lambda$) is calculated at max output power and an operating ambient temperature (T_A) of +40°C. Ericsson Power Modules uses Telcordia SR-332 Issue 2 Method 1 to calculate the mean steady-state failure rate and standard deviation (σ).

Telcordia SR-332 Issue 2 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

Mean steady-state failure rate, λ	Std. deviation, σ
46 nFailures/h	12.4 nFailures/h

MTBF (mean value) for the BMR 642 series = 21.7 Mh.
MTBF at 90% confidence level = 62 Mh

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2002/95/EC and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Ericsson Power Modules products are found in the Statement of Compliance document.

Ericsson Power Modules fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals (REACH) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of the products.

Warranty

Warranty period and conditions are defined in Ericsson Power Modules General Terms and Conditions of Sale.

Limitation of Liability

Ericsson Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

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BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

EN/LZT 146 436 R2A September 2011

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Safety Specification**General information**

Ericsson Power Modules DC/DC converters and DC/DC regulators are designed in accordance with safety standards IEC/EN/UL 60950-1 *Safety of Information Technology Equipment*.

IEC/EN/UL 60950-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Energy hazards
- Fire
- Mechanical and heat hazards
- Radiation hazards
- Chemical hazards

On-board DC/DC converters and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without "Conditions of Acceptability". Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use should comply with the requirements in IEC 60950-1, EN 60950-1 and UL 60950-1 *Safety of Information Technology Equipment*. There are other more product related standards, e.g. IEEE 802.3 CSMA/CD (Ethernet) Access Method, and ETS-300132-2 *Power supply interface at the input to telecommunications equipment, operated by direct current (dc)*, but all of these standards are based on IEC/EN/UL 60950-1 with regards to safety.

Ericsson Power Modules DC/DC converters and DC/DC regulators are UL 60950-1 recognized and certified in accordance with EN 60950-1.

The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

The products should be installed in the end-use equipment, in accordance with the requirements of the ultimate application. Normally the output of the DC/DC converter is considered as SELV (Safety Extra Low Voltage) and the input source must be isolated by minimum Double or Reinforced Insulation from the primary circuit (AC mains) in accordance with IEC/EN/UL 60950-1.

Isolated DC/DC converters

It is recommended that a slow blow fuse is to be used at the input of each DC/DC converter. If an input filter is used in the circuit the fuse should be placed in front of the input filter.

In the rare event of a component problem that imposes a short circuit on the input source, this fuse will provide the following functions:

- Isolate the fault from the input power source so as not to affect the operation of other parts of the system.
- Protect the distribution wiring from excessive current and power loss thus preventing hazardous overheating.

The galvanic isolation is verified in an electric strength test. The test voltage (V_{iso}) between input and output is 1500 Vdc or 2250 Vdc (refer to product specification).

24 V DC systems

The input voltage to the DC/DC converter is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

48 and 60 V DC systems

If the input voltage to the DC/DC converter is 75 Vdc or less, then the output remains SELV (Safety Extra Low Voltage) under normal and abnormal operating conditions.

Single fault testing in the input power supply circuit should be performed with the DC/DC converter connected to demonstrate that the input voltage does not exceed 75 Vdc.

If the input power source circuit is a DC power system, the source may be treated as a TNV-2 circuit and testing has demonstrated compliance with SELV limits in accordance with IEC/EN/UL60950-1.

Non-isolated DC/DC regulators

The input voltage to the DC/DC regulator is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

Input 4.5-14 V, Output up to 12 A / 60 W

$$C_i = 22 \mu F \quad C_o = 100 \mu F$$

BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

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Electrical Specification
BMR 462 0002, BMR 462 1002
 $T_{P1} = -30$ to $+95^{\circ}\text{C}$, $V_I = 4.5$ to 14 V, $V_I > V_O + 1.0$ V

Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12.0$ V, max I_O , unless otherwise specified under Conditions.

Default configuration file, 190 10-CDA 102 0207/001.

External $C_{IN} = 470$ $\mu\text{F}/10$ m Ω , $C_{OUT} = 470$ $\mu\text{F}/10$ m Ω . See Operating Information section for selection of capacitor types.

Sense pins are connected to the output pins.

Characteristics	Conditions	min	typ	max	Unit
V_I	Input voltage rise time			2.4	V/ms

V_O	Output voltage without pin strap		1.2		V
	Output voltage adjustment range	0.60		5.0	V
	Output voltage adjustment including margining	0.54		5.5	V
	Output voltage set-point resolution		± 0.025		% V_O
	Output voltage accuracy	Includes, line, load, temp.	-1	1	%
	Line regulation	$V_O = 0.6$ V	2		mV
		$V_O = 1.0$ V	2		
		$V_O = 3.3$ V	2		
		$V_O = 5.0$ V	3		
	Load regulation; $I_O = 0 - 100\%$	$V_O = 0.6$ V	3		mV
		$V_O = 1.0$ V	2		
		$V_O = 3.3$ V	2		
		$V_O = 5.0$ V	2		
V_{Oac}	Output ripple & noise $C_O = 470$ μF (minimum external capacitance). See Note 12	$V_O = 0.6$ V	20		mVp-p
		$V_O = 1.0$ V	30		
		$V_O = 3.3$ V	60		
		$V_O = 5.0$ V	100		

I_O	Output current		12		A
I_S	Static input current at max I_O	$V_O = 0.6$ V	0,76		A
		$V_O = 1.0$ V	1,17		
		$V_O = 3.3$ V	3,53		
		$V_O = 5.0$ V	4,1		
I_{lim}	Current limit threshold		14	20	A
I_{sc}	Short circuit current	RMS, hiccup mode, See Note 3	$V_O = 0.6$ V	8	A
			$V_O = 1.0$ V	6	
			$V_O = 3.3$ V	5	
			$V_O = 5.0$ V	4	

η	Efficiency	50% of max I _O	V _O = 0.6 V	82.6	%
			V _O = 1.0 V	88,5	
			V _O = 3.3V	94,7	
			V _O = 5.0 V	95,7	
		max I _O	V _O = 0.6 V	78,5	%
			V _O = 1.0 V	85,4	
			V _O = 3.3V	93.6	
			V _O = 5.0 V	94.9	
P _d	Power dissipation at max I _O		V _O = 0.6 V	2.05	W
			V _O = 1.0 V	2.11	
			V _O =3.3V	2.66	
			V _O = 5.0 V	3.15	
P _{ii}	Input idling power (no load)	Default configuration: Continues Conduction Mode, CCM	V _O = 0.6 V	0.33	W
			V _O = 1.0 V	0.35	
			V _O = 3.3V	0.56	
			V _O = 5.0 V	0.99	
P _{CTRL}	Input standby power	Turned off with CTRL-pin	Default configuration: Monitoring enabled, Precise timing enabled	180	mW

Technical Specification

BMR 462 series POL Regulators Input 4.5-14 V, Output up to 12 A / 60 W

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Characteristics		Conditions	min	typ	max	Unit
C_i	Internal input capacitance			22		μF
C_o	Internal output capacitance			100		μF
C_{OUT}	Total external output capacitance	See Note 10	300		7 500	μF
	ESR range of capacitors (per single capacitor)	See Note 10	5		30	m Ω

V_{tr1}	Load transient peak voltage deviation Load step 25-75-25% of max I_o	Default configuration $di/dt = 2 \text{ A}/\mu\text{s}$ $C_o=470 \mu\text{F}$ (minimum external capacitance) see Note 13	$V_o = 0.6 \text{ V}$	55	mV
			$V_o = 1.0 \text{ V}$	65	
			$V_o = 3.3 \text{ V}$	110	
			$V_o = 5.0 \text{ V}$	190	
t_{tr1}	Load transient recovery time, Note 5 Load step 25-75-25% of max I_o	Default configuration $di/dt = 2 \text{ A}/\mu\text{s}$ $C_o=470 \mu\text{F}$ (minimum external capacitance) see Note 13	$V_o = 0.6 \text{ V}$	230	μs
			$V_o = 1.0 \text{ V}$	210	
			$V_o = 3.3 \text{ V}$	200	
			$V_o = 5.0 \text{ V}$	200	

f _s	Switching frequency		320	kHz
	Switching frequency range	PMBus configurable	200-640	kHz
	Switching frequency set-point accuracy		±5	%
	Control Circuit PWM Duty Cycle		595	%
	Minimum Sync Pulse Width		150	ns
	Synchronization Frequency Tolerance	External clock source	-1313	%

Input Under Voltage Lockout, UVLO	UVLO threshold		3.85	V	
	UVLO threshold range	PMBus configurable	3.85-14	V	
	Set point accuracy		-150	150	mV
	UVLO hysteresis		0.35	V	
	UVLO hysteresis range	PMBus configurable	0-10.15	V	
	Delay		2.5	μs	
	Fault response	See Note 3	Automatic restart, 70ms		
Input Over Voltage Protection, IOVP	IOVP threshold		16	V	
	IOVP threshold range	PMBus configurable	4.2-16	V	
	Set point accuracy		-150	150	mV
	IOVP hysteresis		1	V	
	IOVP hysteresis range	PMBus configurable	0-11.8	V	
	Delay		2.5	μs	
	Fault response	See Note 3	Automatic restart, 70ms		
Power Good, PG, See Note 2	PG threshold		90	% V _O	
	PG hysteresis		5	% V _O	
	PG delay		10	ms	
	PG delay range	PMBus configurable	0-500	s	
Output voltage Over/Under Voltage Protection, OVP/UVP	UVP threshold		85	% V _O	
	UVP threshold range	PMBus configurable	0-100	% V _O	
	UVP hysteresis		5	% V _O	
	OVP threshold		115	% V _O	
	OVP threshold range	PMBus configurable	100-115	% V _O	
	UVP/OVP response time		25	μs	
	UVP/OVP response time range	PMBus configurable	5-60	μs	
	Fault response	See Note 3	Automatic restart, 70ms		
Over Current Protection, OCP	OCP threshold		18	A	
	OCP threshold range	PMBus configurable	0-18	A	
	Protection delay, See Note 4		5	T _{SW}	
	Protection delay range	PMBus configurable	1-32	T _{SW}	
	Fault response	See Note 3	Automatic restart, 70ms		

Technical Specification

BMR 462 series POL Regulators Input 4.5-14 V, Output up to 12 A / 60 W

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Characteristics	Conditions	min	typ	max	Unit
Over Temperature Protection, OTP at P1 See Note 9	OTP threshold		120		°C
	OTP threshold range	PMBus configurable	-40...+120		°C
	OTP hysteresis		15		°C
	OTP hysteresis range	PMBus configurable	0-160		°C
	Fault response	See Note 3	Automatic restart, 70ms		

V _{IL}	Logic input low threshold	SYNC, SA0, SA1, SCL, SDA, GCB, CTRL, VSET		0.8	V
V _{IH}	Logic input high threshold		2		V
I _{IL}	Logic input low sink current	CTRL		0.6	mA
V _{OL}	Logic output low			0.4	V
V _{OH}	Logic output high	SYNC, SCL, SDA, SALERT, GCB, PG	2.25		V
I _{OL}	Logic output low sink current			4	mA
I _{OH}	Logic output high source current			2	mA
t _{set}	Setup time, SMBus	See Note 1	300		ns
t _{hold}	Hold time, SMBus	See Note 1	250		ns
t _{free}	Bus free time, SMBus	See Note 1	2		ms
C _p	Internal capacitance on logic pins			10	pF

Start-Up time		See Note 11	30		ms
Output Voltage Delay Time See Note 6	Delay duration		10		ms
	Delay duration range	PMBus configurable	2-500000		
	Delay accuracy	Default configuration: CTRL controlled Precise timing enabled	±0.25		ms
		PMBus controlled Precise timing disabled	-0.25/+4		ms
Output Voltage Ramp Time	Ramp duration		10		ms
	Ramp duration range	PMBus configurable	0-200		
	Ramp time accuracy		100		µs

VTRK Input Bias Current	V _{VTRK} = 5.5 V		110	200	µA
VTRK Tracking Ramp Accuracy, Note 8	100% Tracking (V _O - V _{VTRK})	-100		100	mV
VTRK Regulation Accuracy	100% Tracking (V _O - V _{VTRK})	-1		1	%

VIN_READ, 0x88h	Accuracy vs. V _I		3		%
VOUT_READ, 0x8Bh	Accuracy vs. V _O		1		%
IOUT_READ, 0x8Ch	Accuracy vs. I _O	I _O = 0-12 A, T _{P1} = 0 to +95°C V _I = 12 V	±1.6		A
IOUT_READ, 0x8Ch	Accuracy vs. I _O	I _O = 0-12 A, T _{P1} = 0 to +95°C V _I = 4.5-14 V	±2.7		A

Note 1: See section I2C/SMBus Setup and Hold Times – Definitions.

Note 2: Monitorable over PMBus Interface.

Note 3: Continuous re-starts with 70 ms between each start. See Power Management section for additional fault response types.

Note 4: T_{sw} is the switching period.

Note 5: Within +/-5% of V_O

Note 6: See section Soft-start Power Up.

Note 8: Tracking functionality is designed to follow a VTRK signal with slewrates < 2.4V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.

Note 9: See section Over Temperature Protection (OTP).

Note 10: See section External Capacitors.

Note 11: See section Start-Up Procedure.

Note 12: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.

Note 13: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.

BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

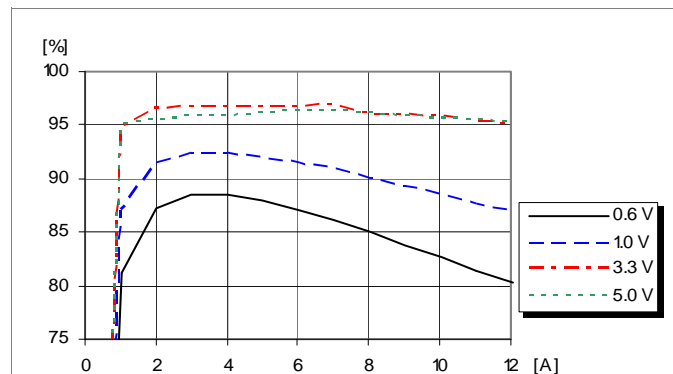
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Typical Characteristics Efficiency and Power Dissipation

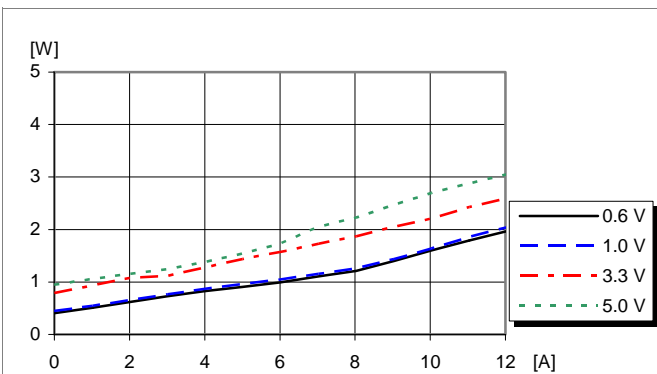
BMR 462 0002, BMR 462 1002

Efficiency vs. Output Current, $V_I=5\text{ V}$



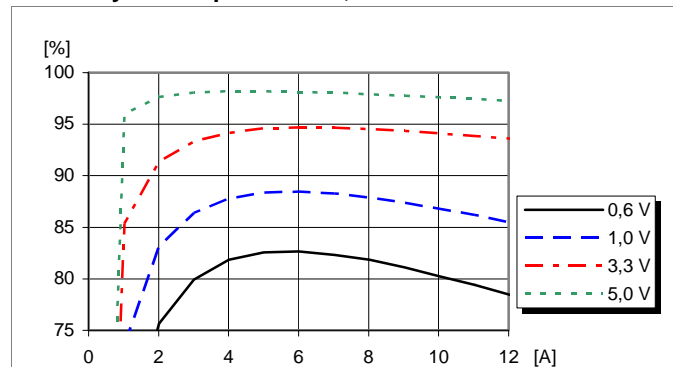
Efficiency vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=5\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Power Dissipation vs. Output Current, $V_I=5\text{ V}$



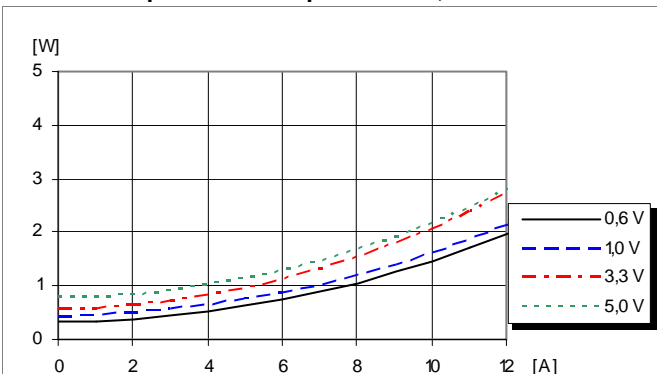
Dissipated power vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=5\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Efficiency vs. Output Current, $V_I=12\text{ V}$



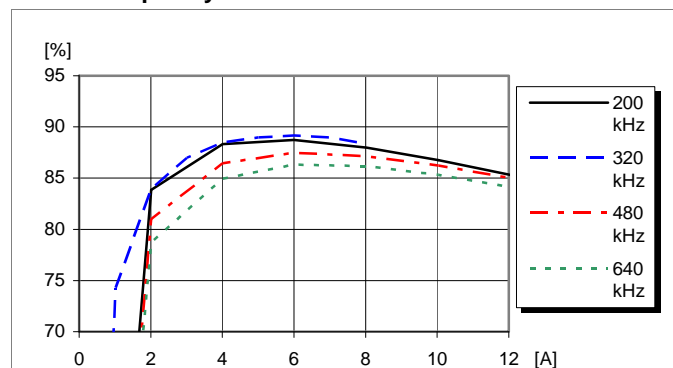
Efficiency vs. load current and output voltage at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Power Dissipation vs. Output Current, $V_I=12\text{ V}$



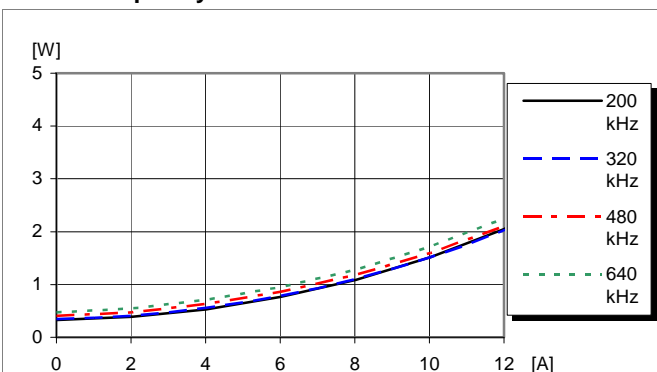
Dissipated power vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Efficiency vs. Output Current and Switch Frequency



Efficiency vs. load current and switch frequency at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $V_O=3.3\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
Default configuration except changed frequency

Power Dissipation vs. Output Current and Switch frequency



Dissipated power vs. load current and switch frequency at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $V_O=3.3\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
Default configuration except changed frequency

BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

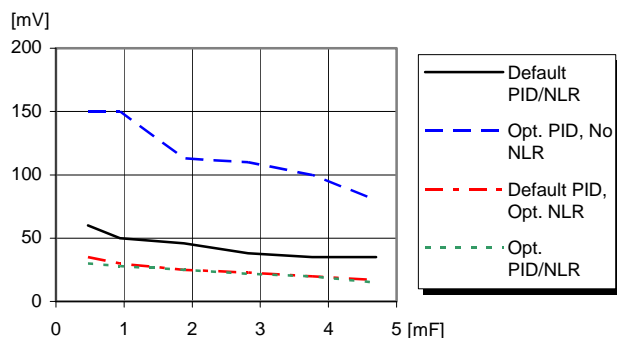
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Typical Characteristics Load Transient

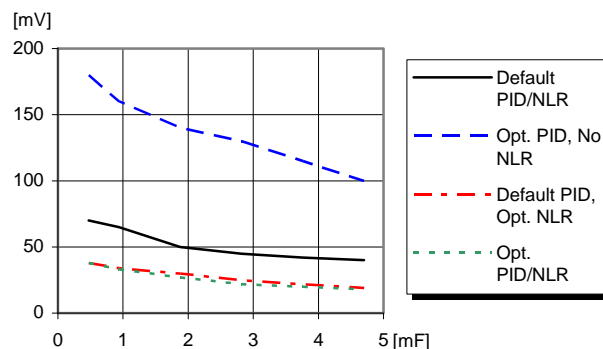
BMR 462 0002, BMR 462 1002

Load Transient vs. External Capacitance, $V_O=1.0$ V



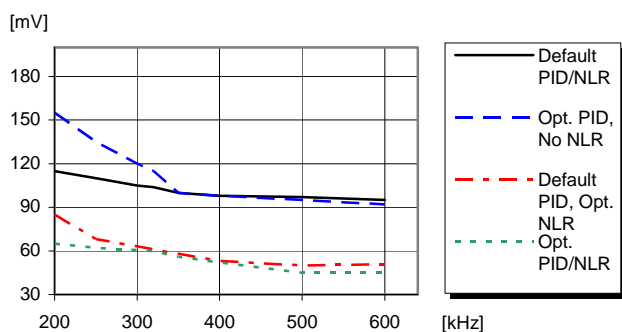
Load transient peak voltage deviation vs. external capacitance.
Step-change (3-9-3 A). Parallel coupling of capacitors with 470 μ F/10 m Ω ,
 $T_{P1} = +25^\circ\text{C}$. $V_I=12$ V, $V_O=1.0$ V, $f_{sw}=320$ kHz, $di/dt=2$ A/ μ s

Load Transient vs. External Capacitance, $V_O=3.3$ V



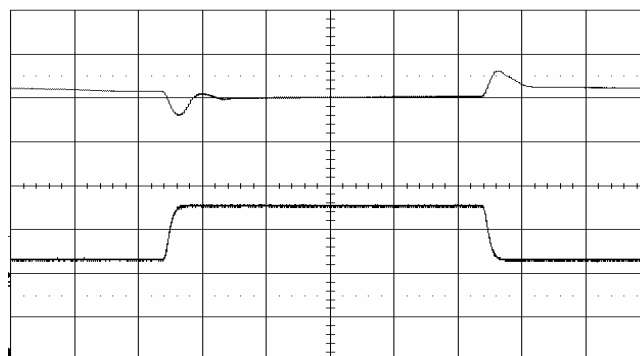
Load transient peak voltage deviation vs. external capacitance.
Step-change (3-9-3 A). Parallel coupling of capacitors with 470 μ F/10 m Ω ,
 $T_{P1} = +25^\circ\text{C}$. $V_I=12$ V, $V_O=3.3$ V, $f_{sw}=320$ kHz, $di/dt=2$ A/ μ s

Load transient vs. Switch Frequency



Load transient peak voltage deviation vs. frequency.
Step-change (3-9-3 A).
 $T_{P1} = +25^\circ\text{C}$. $V_I=12$ V, $V_O=3.3$ V, $C_O=470$ μ F/10 m Ω

Output Load Transient Response, Default PID/NLR



Output voltage response to load current step-change (3-9-3 A) at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12$ V, $V_O = 3.3$ V
 $di/dt=2$ A/ μ s, $f_{sw}=320$ kHz, $C_O=470$ μ F/10 m Ω

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

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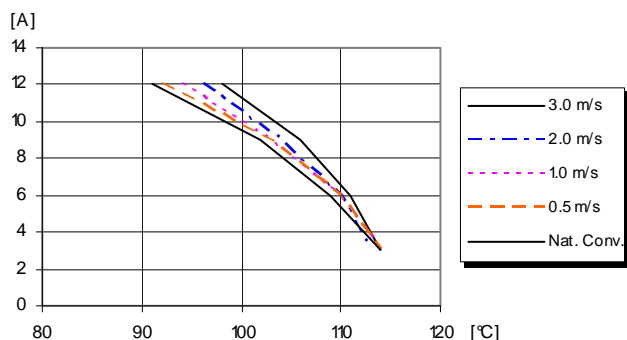
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Typical Characteristics

Output Current Characteristic

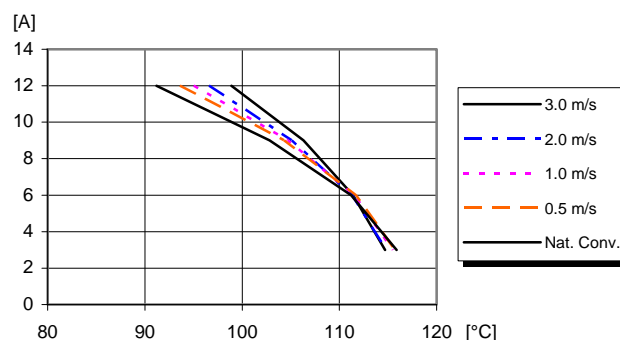
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Output Current Derating, $V_O=0.6\text{ V}$



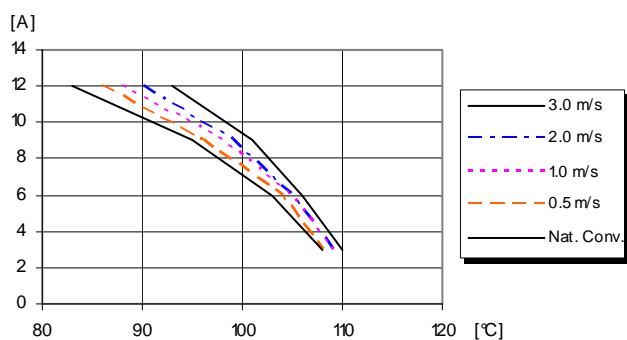
Available load current vs. ambient air temperature and airflow at $V_O=0.6\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Output Current Derating, $V_O=1.0\text{ V}$



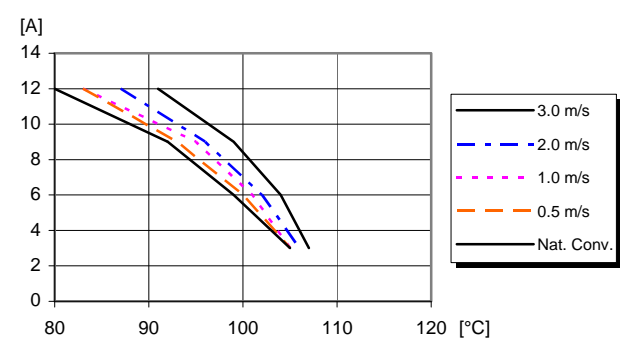
Available load current vs. ambient air temperature and airflow at $V_O=1.0\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Output Current Derating, $V_O=3.3\text{ V}$



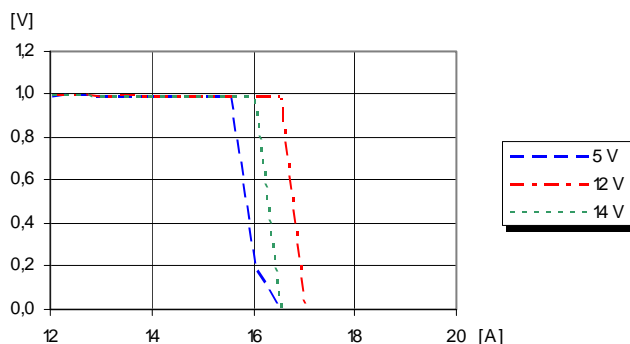
Available load current vs. ambient air temperature and airflow at $V_O=3.3\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Output Current Derating, $V_O=5.0\text{ V}$



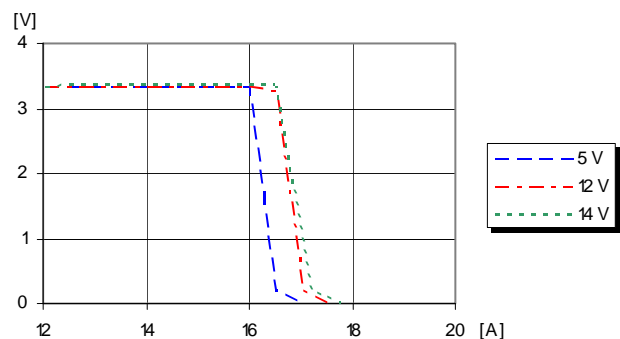
Available load current vs. ambient air temperature and airflow at $V_O=5.0\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Current Limit Characteristics, $V_O=1.0\text{ V}$



Output voltage vs. load current at $T_{P1} = +25^\circ\text{C}$. $V_O=1.0\text{ V}$.

Current Limit Characteristics, $V_O=3.3\text{ V}$



Output voltage vs. load current at $T_{P1} = +25^\circ\text{C}$. $V_O=3.3\text{ V}$.

BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

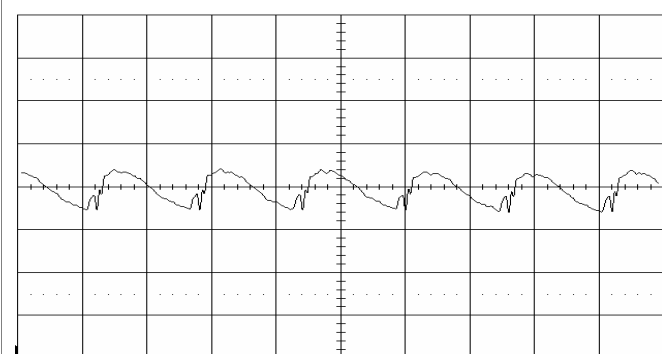
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Typical Characteristics Output Voltage

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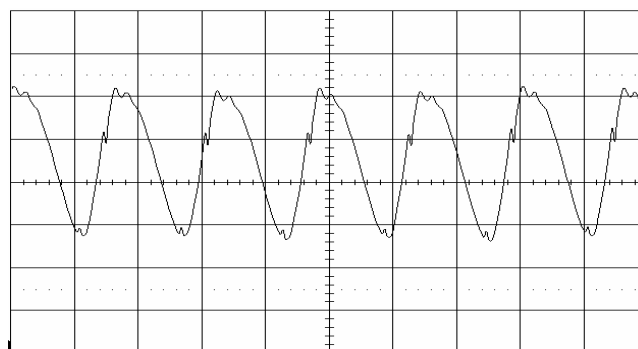
Output Ripple & Noise, $V_O=1.0$ V



Output voltage ripple at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12$ V, $C_O = 470$ $\mu\text{F}/10$ m Ω
 $I_O = 12$ A resistive load

Trace: output voltage (20 mV/div.).
Time scale: (2 $\mu\text{s}/\text{div.}$).

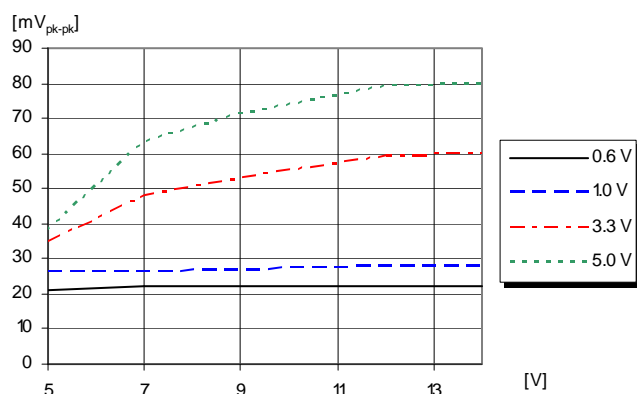
Output Ripple & Noise, $V_O=3.3$ V



Output voltage ripple at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12$ V, $C_O = 470$ $\mu\text{F}/10$ m Ω
 $I_O = 12$ A resistive load

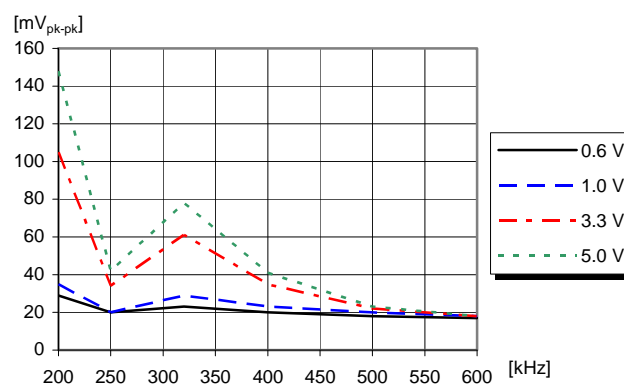
Trace: output voltage (20 mV/div.).
Time scale: (2 $\mu\text{s}/\text{div.}$).

Output Ripple vs. Input Voltage



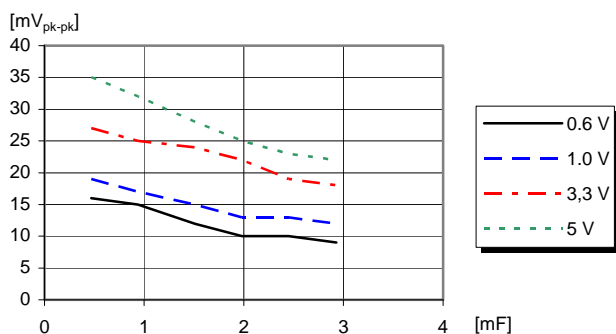
Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $C_O = 470$ $\mu\text{F}/10$ m Ω ,
 $I_O = 12$ A resistive load.

Output Ripple vs. Frequency



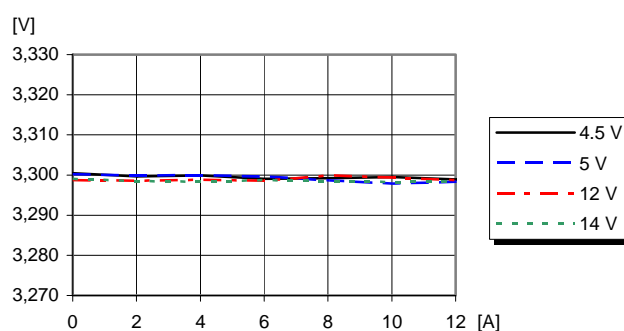
Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $V_I = 12$ V, $C_O = 470$ $\mu\text{F}/10$ m Ω ,
 $I_O = 12$ A resistive load. Default configuration except changed frequency.

Output Ripple vs. External Capacitance



Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $V_I = 12$ V, $I_O = 12$ A resistive load.
Parallel coupling of capacitors with 470 $\mu\text{F}/10$ m Ω ,

Load regulation, $V_O=3.3$ V



Load regulation at $V_O=3.3$ V at: $T_{P1} = +25^\circ\text{C}$, $C_O = 470$ $\mu\text{F}/10$ m Ω

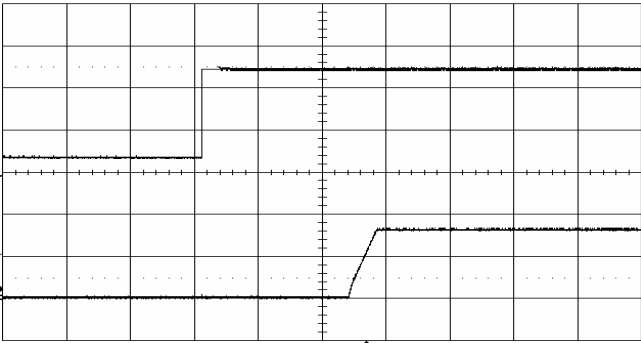
BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

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Typical Characteristics
Start-up and shut-down

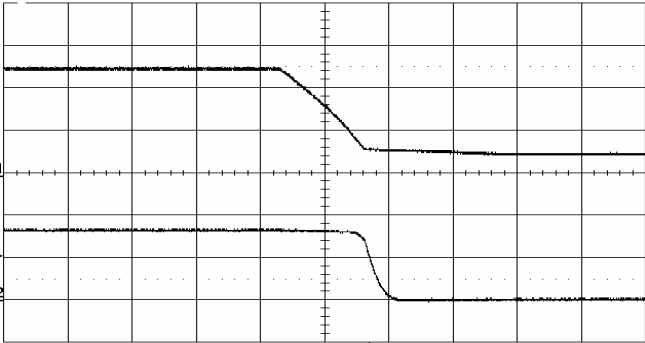
BMR 462 0002, BMR 462 1002

Start-up by input source



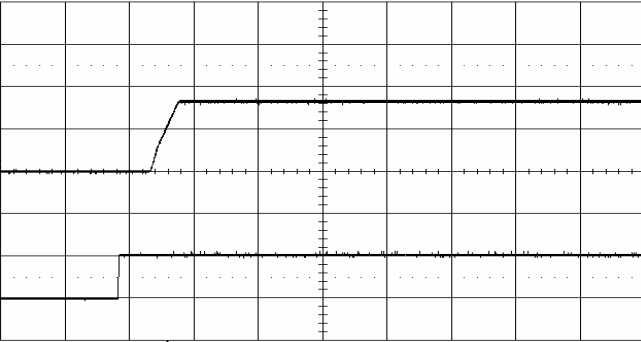
Start-up enabled by connecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 12\text{ A}$ resistive load
Top trace: Input voltage (5 V/div.).
Bottom trace: Output voltage (2 V/div.).
Time scale: (20 ms/div.).

Shut-down by input source



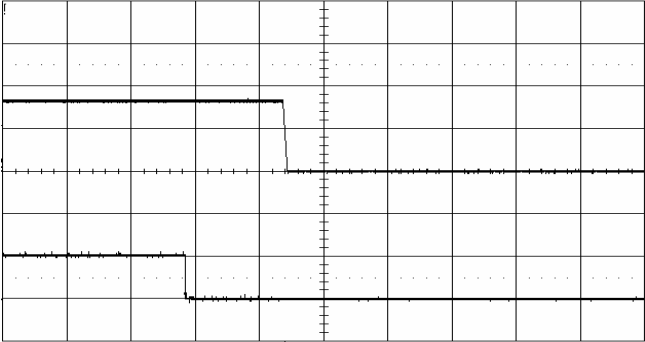
Shut-down enabled by disconnecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 12\text{ A}$ resistive load
Top trace: Input voltage (5 V/div.).
Bottom trace: Output voltage (2 V/div.).
Time scale: (2 ms/div.).

Start-up by CTRL signal



Start-up by enabling CTRL signal at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 12\text{ A}$ resistive load
Top trace: output voltage (2 V/div.).
Bottom trace: CTRL signal (2 V/div.).
Time scale: (20 ms/div.).

Shut-down by CTRL signal



Shut-down enabled by disconnecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 12\text{ A}$ resistive load
Top trace: output voltage (2 V/div.).
Bottom trace: CTRL signal (2 V/div.).
Time scale: (2 ms/div.).

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 $T_{P1} = -30$ to $+95^{\circ}\text{C}$, $V_I = 4.5$ to 14 V , $V_I > V_O + 1.0\text{ V}$

Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12.0\text{ V}$, max I_O , unless otherwise specified under Conditions.

Default configuration file, 190 10-CDA 102 0260/001.

External $C_{IN} = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $C_{OUT} = 470\text{ }\mu\text{F}/10\text{ m}\Omega$. See Operating Information section for selection of capacitor types.

Sense pins are connected to the output pins.

Characteristics	Conditions	min	typ	max	Unit
V_I	Input voltage rise time			2.4	V/ms

V_O	Output voltage without pin strap		1.2		V
	Output voltage adjustment range	0.60		5.0	V
	Output voltage adjustment including margining	0.54		5.5	V
	Output voltage set-point resolution		± 0.025		% V_O
	Output voltage accuracy	Includes, line, load, temp.	-1	1	%
	Line regulation	$V_O = 0.6\text{ V}$	2		mV
		$V_O = 1.0\text{ V}$	2		
		$V_O = 3.3\text{ V}$	2		
		$V_O = 5.0\text{ V}$	3		
	Load regulation; $I_O = 0 - 100\%$	$V_O = 0.6\text{ V}$	3		mV
		$V_O = 1.0\text{ V}$	2		
		$V_O = 3.3\text{ V}$	2		
		$V_O = 5.0\text{ V}$	2		
V_{Oac}	Output ripple & noise $C_O = 470\text{ }\mu\text{F}$ (minimum external capacitance). See Note 12	$V_O = 0.6\text{ V}$	20		mVp-p
		$V_O = 1.0\text{ V}$	30		
		$V_O = 3.3\text{ V}$	55		
		$V_O = 5.0\text{ V}$	95		

I_O	Output current		12		A
I_S	Static input current at max I_O	$V_O = 0.6\text{ V}$	0,75		A
		$V_O = 1.0\text{ V}$	1,21		
		$V_O = 3.3\text{ V}$	3,55		
		$V_O = 5.0\text{ V}$	4,1		
I_{lim}	Current limit threshold		14	20	A
I_{sc}	Short circuit current	RMS, hiccup mode, See Note 3	$V_O = 0.6\text{ V}$	8	A
			$V_O = 1.0\text{ V}$	6	
			$V_O = 3.3\text{ V}$	5	
			$V_O = 5.0\text{ V}$	4	

η	Efficiency	50% of max I_O	$V_O = 0.6\text{ V}$	81.4	%
			$V_O = 1.0\text{ V}$	88.1	
			$V_O = 3.3\text{ V}$	95.9	
			$V_O = 5.0\text{ V}$	97.2	
		max I_O	$V_O = 0.6\text{ V}$	78.8	%
			$V_O = 1.0\text{ V}$	85.8	
			$V_O = 3.3\text{ V}$	95.1	
			$V_O = 5.0\text{ V}$	96.8	
P_d	Power dissipation at max I_O		$V_O = 0.6\text{ V}$	1.90	W
			$V_O = 1.0\text{ V}$	1.97	
			$V_O = 3.3\text{ V}$	2.65	
			$V_O = 5.0\text{ V}$	3.12	
P_{ii}	Input idling power (no load)	Default configuration: Continues Conduction Mode, CCM	$V_O = 0.6\text{ V}$	0.36	W
			$V_O = 1.0\text{ V}$	0.35	
			$V_O = 3.3\text{ V}$	0.54	
			$V_O = 5.0\text{ V}$	0.97	
P_{CTRL}	Input standby power	Turned off with CTRL-pin	Default configuration: Monitoring enabled, Precise timing enabled	180	mW

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Characteristics		Conditions	min	typ	max	Unit
C_i	Internal input capacitance			22		μF
C_o	Internal output capacitance			100		μF
C_{OUT}	Total external output capacitance	See Note 10	300		7 500	μF
	ESR range of capacitors (per single capacitor)	See Note 10	5		30	m Ω

V_{tr1}	Load transient peak voltage deviation	Default configuration $di/dt = 2 \text{ A}/\mu\text{s}$ $C_o=470 \mu\text{F}$ (minimum external capacitance) see Note 13	$V_o = 0.6 \text{ V}$	50	mV
			$V_o = 1.0 \text{ V}$	60	
			$V_o = 3.3 \text{ V}$	105	
			$V_o = 5.0 \text{ V}$	190	
t_{tr1}	Load transient recovery time, Note 5	Default configuration $di/dt = 2 \text{ A}/\mu\text{s}$ $C_o=470 \mu\text{F}$ (minimum external capacitance) see Note 13	$V_o = 0.6 \text{ V}$	230	μs
			$V_o = 1.0 \text{ V}$	205	
			$V_o = 3.3 \text{ V}$	195	
			$V_o = 5.0 \text{ V}$	200	

f _s	Switching frequency		320	kHz
	Switching frequency range	PMBus configurable	200-640	kHz
	Switching frequency set-point accuracy		±5	%
	Control Circuit PWM Duty Cycle		595	%
	Minimum Sync Pulse Width		150	ns
	Synchronization Frequency Tolerance	External clock source	-1313	%

Input Under Voltage Lockout, UVLO	UVLO threshold		3.85	V
	UVLO threshold range	PMBus configurable	3.85-14	V
	Set point accuracy		-150150	mV
	UVLO hysteresis		0.35	V
	UVLO hysteresis range	PMBus configurable	0-10.15	V
	Delay		2.5	μs
	Fault response	See Note 3	Automatic restart, 70ms	
Input Over Voltage Protection, IOVP	IOVP threshold		16	V
	IOVP threshold range	PMBus configurable	4.2-16	V
	Set point accuracy		-150150	mV
	IOVP hysteresis		1	V
	IOVP hysteresis range	PMBus configurable	0-11.8	V
	Delay		2.5	μs
	Fault response	See Note 3	Automatic restart, 70ms	
Power Good, PG, See Note 2	PG threshold		90	% V _O
	PG hysteresis		5	% V _O
	PG delay		10	ms
	PG delay range	PMBus configurable	0-500	S
Output voltage Over/Under Voltage Protection, OVP/UVP	UVP threshold		85	% V _O
	UVP threshold range	PMBus configurable	0-100	% V _O
	UVP hysteresis		5	% V _O
	OVP threshold		115	% V _O
	OVP threshold range	PMBus configurable	100-115	% V _O
	UVP/OVP response time		25	μs
	UVP/OVP response time range	PMBus configurable	5-60	μs
	Fault response	See Note 3	Automatic restart, 70ms	
Over Current Protection, OCP	OCP threshold		18	A
	OCP threshold range	PMBus configurable	0-18	A
	Protection delay, See Note 4		5	T _{sw}
	Protection delay range	PMBus configurable	1-32	T _{sw}
	Fault response	See Note 3	Automatic restart, 70ms	

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Characteristics	Conditions	min	typ	max	Unit
Over Temperature Protection, OTP at P1 See Note 9	OTP threshold		120		°C
	OTP threshold range	PMBus configurable	-40...+120		°C
	OTP hysteresis		15		°C
	OTP hysteresis range	PMBus configurable	0-160		°C
	Fault response	See Note 3	Automatic restart, 70ms		

V _{IL}	Logic input low threshold	SYNC, SA0, SA1, SCL, SDA, GCB, CTRL, VSET		0.8	V
V _{IH}	Logic input high threshold		2		V
I _{IL}	Logic input low sink current	CTRL		0.6	mA
V _{OL}	Logic output low			0.4	V
V _{OH}	Logic output high	SYNC, SCL, SDA, SALERT, GCB, PG	2.25		V
I _{OL}	Logic output low sink current			4	mA
I _{OH}	Logic output high source current			2	mA
t _{set}	Setup time, SMBus	See Note 1	300		ns
t _{hold}	Hold time, SMBus	See Note 1	250		ns
t _{free}	Bus free time, SMBus	See Note 1	2		ms
C _p	Internal capacitance on logic pins			10	pF

Start-Up time		See Note 11	30		ms
Output Voltage Delay Time See Note 6	Delay duration		10		ms
	Delay duration range	PMBus configurable	2-500000		
	Delay accuracy	Default configuration: CTRL controlled Precise timing enabled	±0.25		ms
		PMBus controlled Precise timing disabled	-0.25/+4		ms
Output Voltage Ramp Time	Ramp duration		10		ms
	Ramp duration range	PMBus configurable	0-200		
	Ramp time accuracy		100		µs

VTRK Input Bias Current	V _{VTRK} = 5.5 V		110	200	µA
VTRK Tracking Ramp Accuracy, Note 8	100% Tracking (V _O - V _{VTRK})	-100		100	mV
VTRK Regulation Accuracy	100% Tracking (V _O - V _{VTRK})	-1		1	%

VIN_READ, 0x88h	Accuracy vs. V _I		3		%
VOUT_READ, 0x8Bh	Accuracy vs. V _O		1		%
IOUT_READ, 0x8Ch	Accuracy vs. I _O	I _O = 0-12 A, T _{P1} = 0 to +95°C V _I = 12 V	±1.6		A
IOUT_READ, 0x8Ch	Accuracy vs. I _O	I _O = 0-12 A, T _{P1} = 0 to +95°C V _I = 4.5-14 V	±2.7		A

Note 1: See section I2C/SMBus Setup and Hold Times – Definitions.

Note 2: Monitorable over PMBus Interface.

Note 3: Continuous re-starts with 70 ms between each start. See Power Management section for additional fault response types.

Note 4: T_{sw} is the switching period.

Note 5: Within +/-5% of V_O.

Note 6: See section Soft-start Power Up.

Note 8: Tracking functionality is designed to follow a VTRK signal with slewrates < 2.4V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.

Note 9: See section Over Temperature Protection (OTP).

Note 10: See section External Capacitors.

Note 11: See section Start-Up Procedure.

Note 12: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.

Note 13: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.

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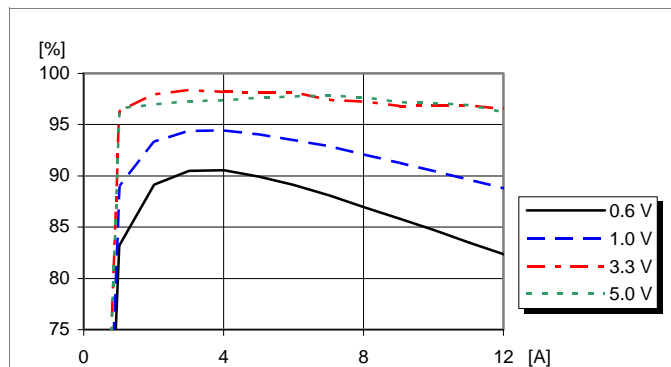
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Typical Characteristics Efficiency and Power Dissipation

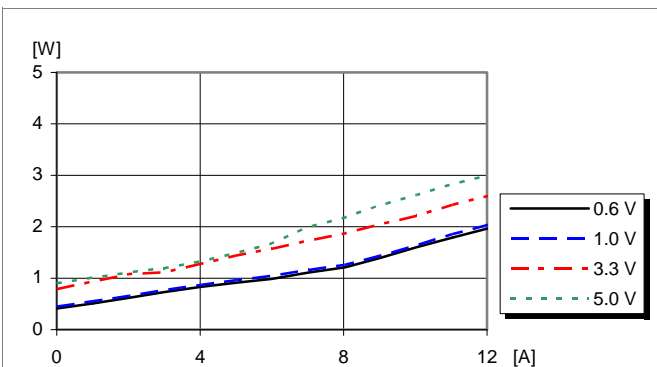
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Efficiency vs. Output Current, $V_I=5\text{ V}$



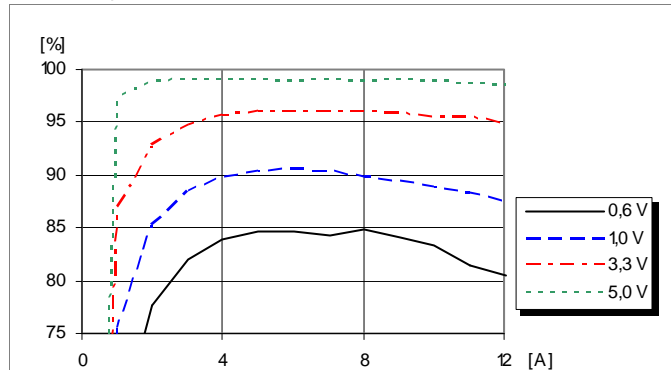
Efficiency vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=5\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Power Dissipation vs. Output Current, $V_I=5\text{ V}$



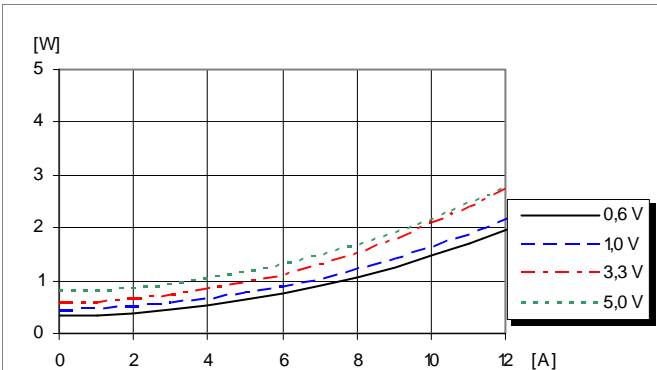
Dissipated power vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=5\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Efficiency vs. Output Current, $V_I=12\text{ V}$



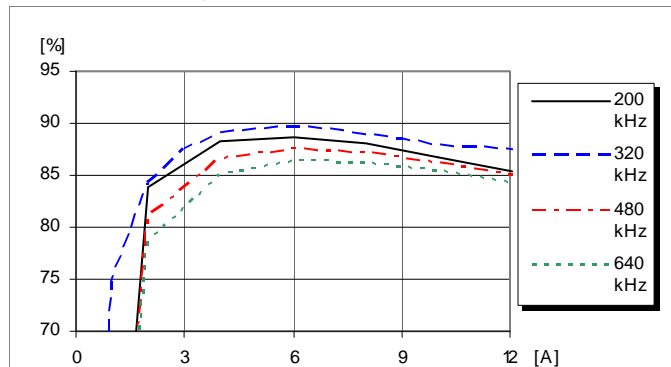
Efficiency vs. load current and output voltage at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Power Dissipation vs. Output Current, $V_I=12\text{ V}$



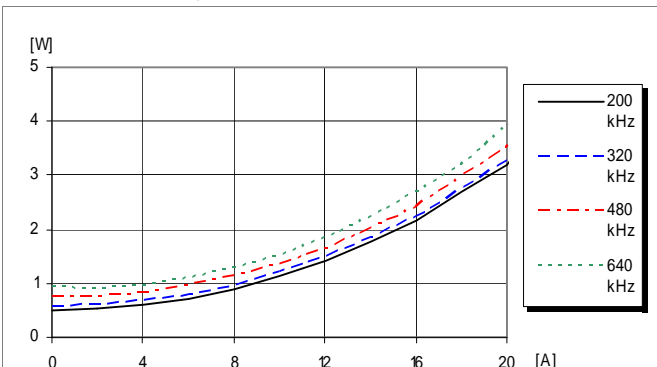
Dissipated power vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Efficiency vs. Output Current and Switch Frequency



Efficiency vs. load current and switch frequency at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $V_O=3.3\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
Default configuration except changed frequency

Power Dissipation vs. Output Current and Switch frequency



Dissipated power vs. load current and switch frequency at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $V_O=3.3\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
Default configuration except changed frequency

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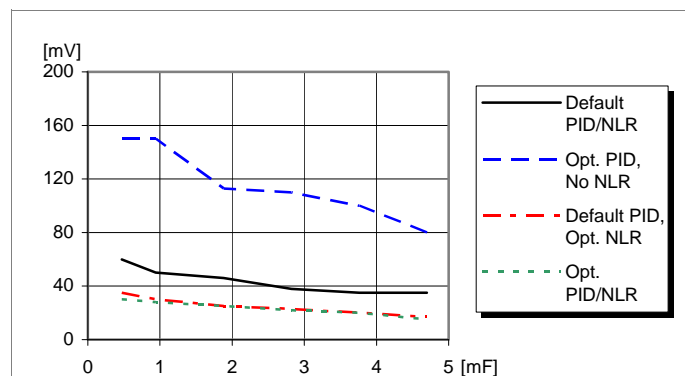
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Typical Characteristics

Load Transient

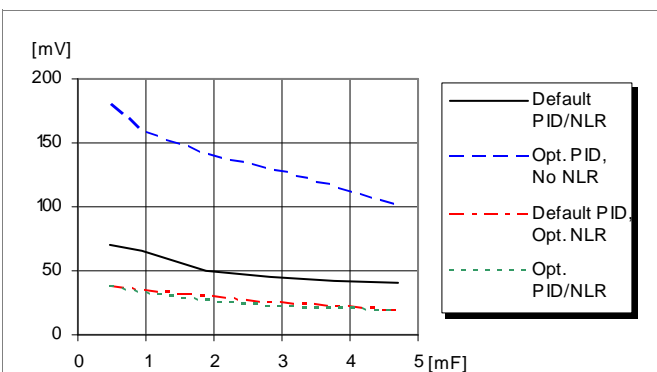
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Load Transient vs. External Capacitance, $V_O=1.0$ V



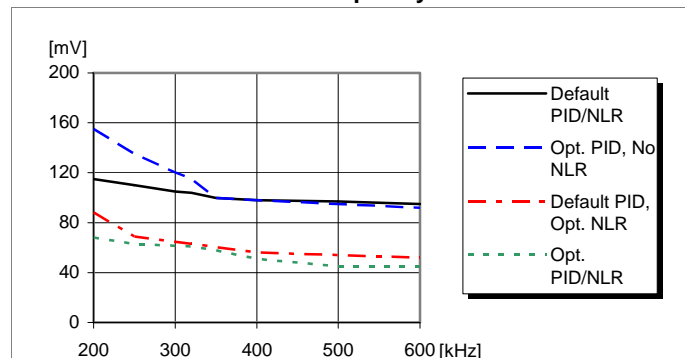
Load transient peak voltage deviation vs. external capacitance.
Step-change (3-9-3 A). Parallel coupling of capacitors with 470 μ F/10 m Ω ,
 $T_{P1} = +25^\circ\text{C}$. $V_I=12$ V, $V_O=1.0$ V, $f_{sw}=320$ kHz, $di/dt=2$ A/ μ s

Load Transient vs. External Capacitance, $V_O=3.3$ V



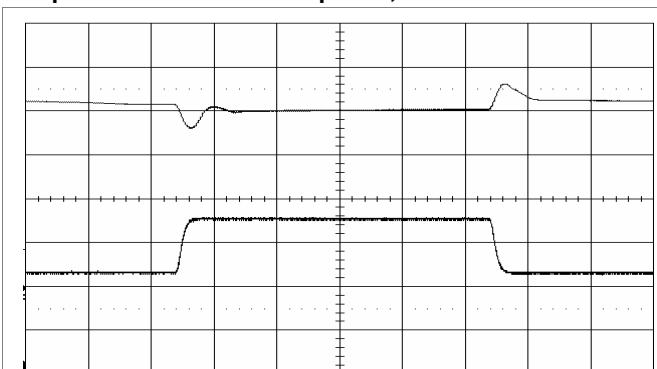
Load transient peak voltage deviation vs. external capacitance.
Step-change (3-9-3 A). Parallel coupling of capacitors with 470 μ F/10 m Ω ,
 $T_{P1} = +25^\circ\text{C}$. $V_I=12$ V, $V_O=3.3$ V, $f_{sw}=320$ kHz, $di/dt=2$ A/ μ s

Load transient vs. Switch Frequency



Load transient peak voltage deviation vs. frequency.
Step-change (3-9-3 A).
 $T_{P1} = +25^\circ\text{C}$. $V_I=12$ V, $V_O=3.3$ V, $C_O=470$ μ F/10 m Ω

Output Load Transient Response, Default PID/NLR



Output voltage response to load current step-change (3-9-3 A) at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12$ V, $V_O = 3.3$ V
 $di/dt=2$ A/ μ s, $f_{sw}=320$ kHz, $C_O=470$ μ F/10 m Ω

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (10 A/div.).
Time scale: (0.1 ms/div.).

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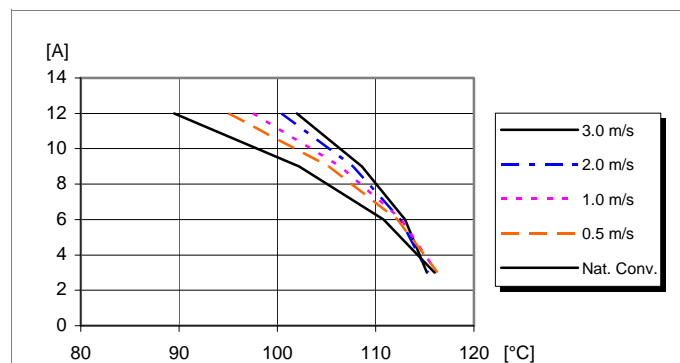
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Typical Characteristics

Output Current Characteristic

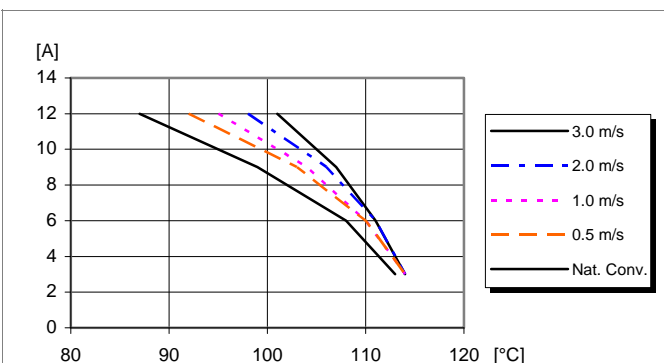
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Output Current Derating, $V_O=0.6\text{ V}$



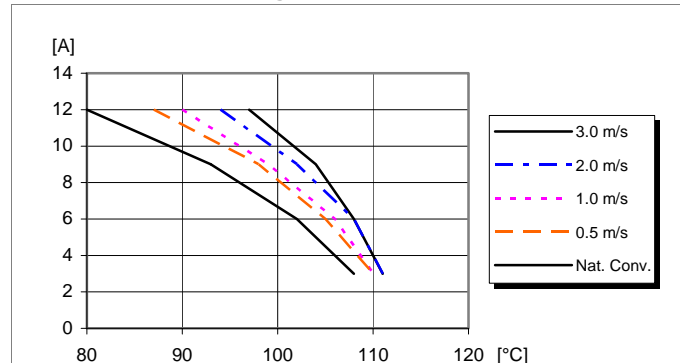
Available load current vs. ambient air temperature and airflow at $V_O=0.6\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Output Current Derating, $V_O=1.0\text{ V}$



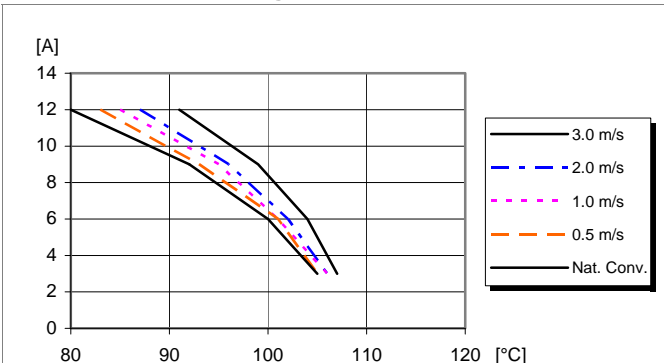
Available load current vs. ambient air temperature and airflow at $V_O=1.0\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Output Current Derating, $V_O=3.3\text{ V}$



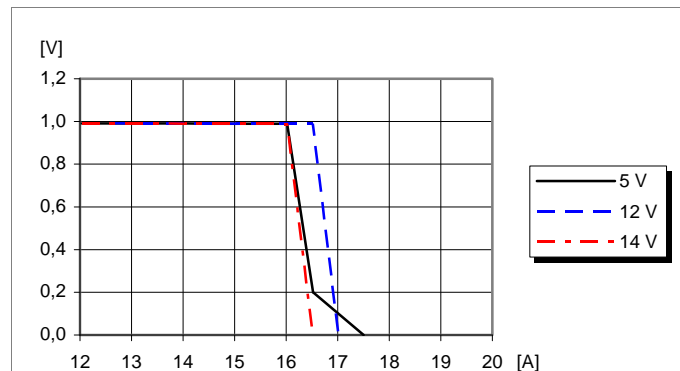
Available load current vs. ambient air temperature and airflow at $V_O=3.3\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Output Current Derating, $V_O=5.0\text{ V}$



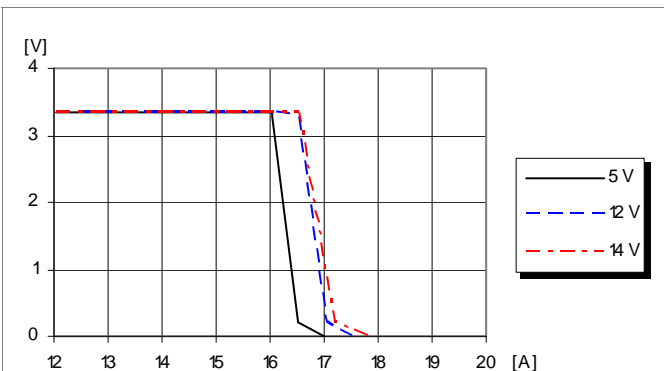
Available load current vs. ambient air temperature and airflow at $V_O=5.0\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Current Limit Characteristics, $V_O=1.0\text{ V}$



Output voltage vs. load current at $T_{P1} = +25^\circ\text{C}$. $V_O=1.0\text{ V}$.

Current Limit Characteristics, $V_O=3.3\text{ V}$



Output voltage vs. load current at $T_{P1} = +25^\circ\text{C}$. $V_O=3.3\text{ V}$.

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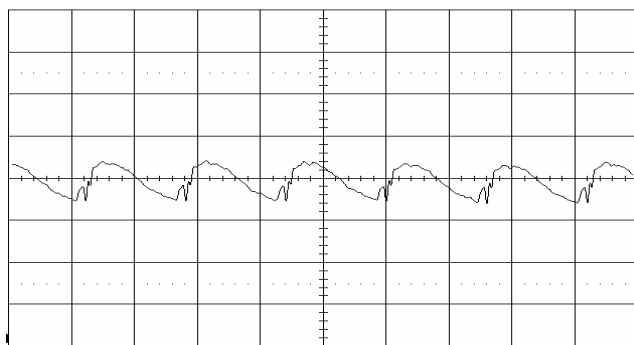
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Typical Characteristics

Output Voltage

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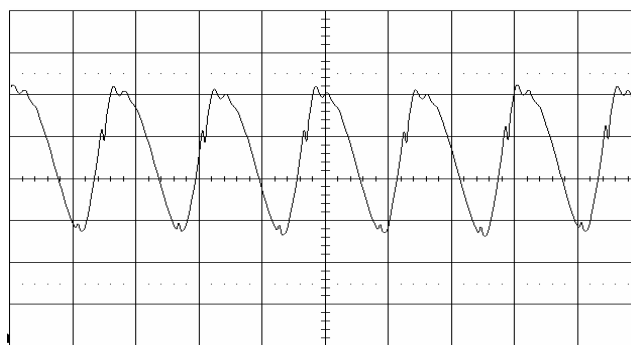
Output Ripple & Noise, $V_O=1.0\text{ V}$



Output voltage ripple at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$
 $I_O = 12\text{ A}$ resistive load

Trace: output voltage (10 mV/div.).
Time scale: (2 $\mu\text{s}/\text{div.}$).

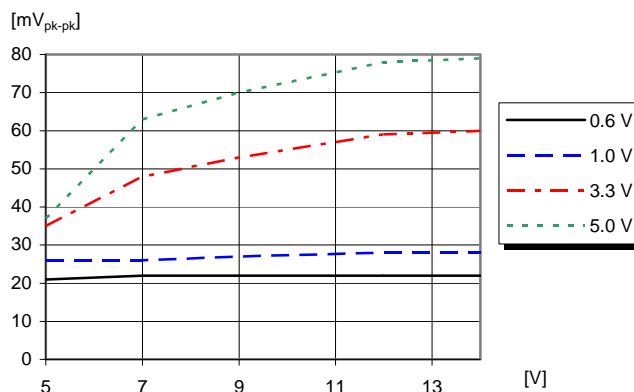
Output Ripple & Noise, $V_O=3.3\text{ V}$



Output voltage ripple at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$
 $I_O = 12\text{ A}$ resistive load

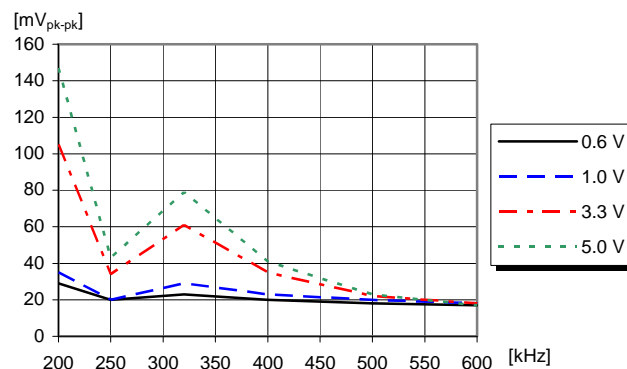
Trace: output voltage (10 mV/div.).
Time scale: (2 $\mu\text{s}/\text{div.}$).

Output Ripple vs. Input Voltage



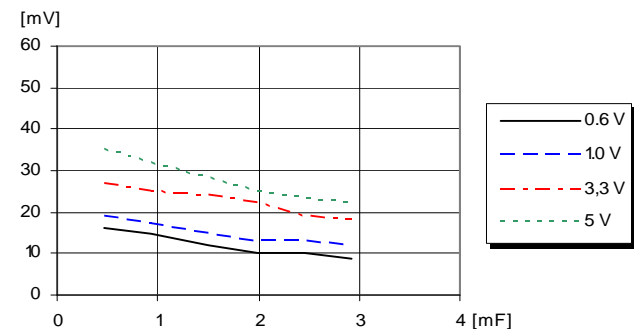
Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$,
 $I_O = 12\text{ A}$ resistive load.

Output Ripple vs. Frequency



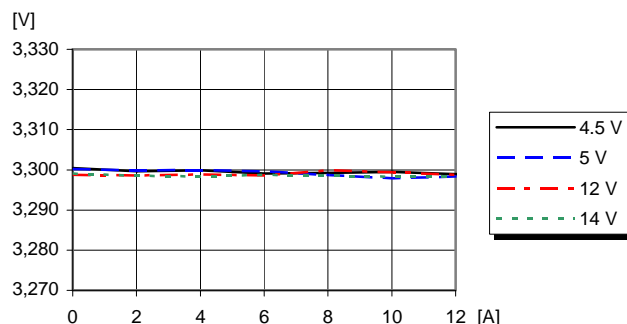
Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$,
 $I_O = 12\text{ A}$ resistive load. Default configuration except changed frequency.

Output Ripple vs. External Capacitance



Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $I_O = 12\text{ A}$ resistive load.
Parallel coupling of capacitors with $470\text{ }\mu\text{F}/10\text{ m}\Omega$,

Load regulation, $V_O=3.3\text{ V}$



Load regulation at $V_O=3.3\text{ V}$ at: $T_{P1} = +25^\circ\text{C}$, $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$

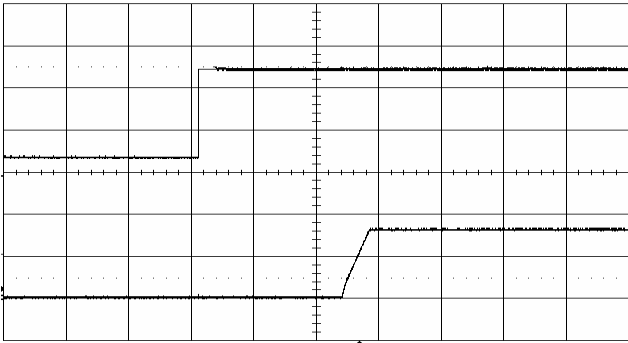
BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

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Typical Characteristics
Start-up and shut-down

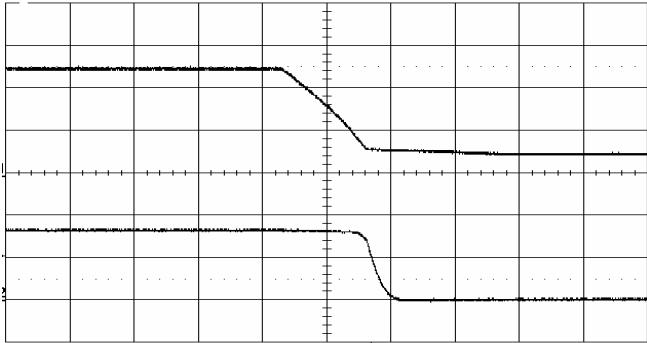
BMR 462 2002 (SIP)

Start-up by input source



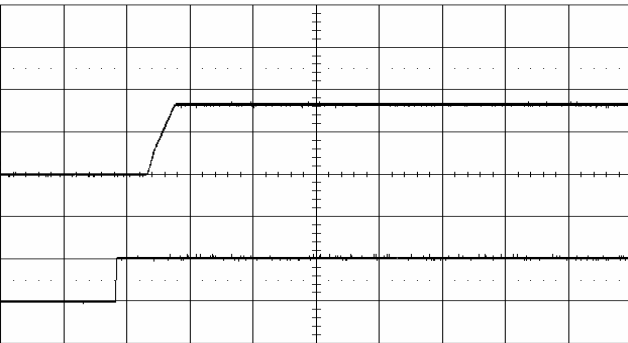
Start-up enabled by connecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 12\text{ A}$ resistive load
Top trace: Input voltage (5 V/div.).
Bottom trace: Output voltage (2 V/div.).
Time scale: (20 ms/div.).

Shut-down by input source



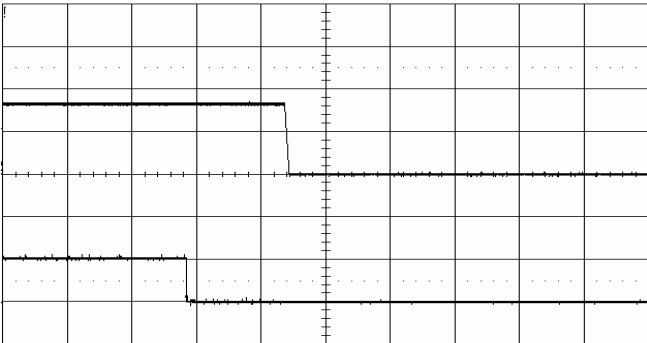
Shut-down enabled by disconnecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 12\text{ A}$ resistive load
Top trace: Input voltage (5 V/div.).
Bottom trace: Output voltage (2 V/div.).
Time scale: (2 ms/div.).

Start-up by CTRL signal



Start-up enabled by connecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 12\text{ A}$ resistive load
Top trace: output voltage (2 V/div.).
Bottom trace: CTRL signal (2 V/div.).
Time scale: (20 ms/div.).

Shut-down by CTRL signal



Shut-down enabled by disconnecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 12\text{ A}$ resistive load
Top trace: output voltage (2 V/div.).
Bottom trace: CTRL signal (2 V/div.).
Time scale: (2 ms/div.).

Technical Specification

BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

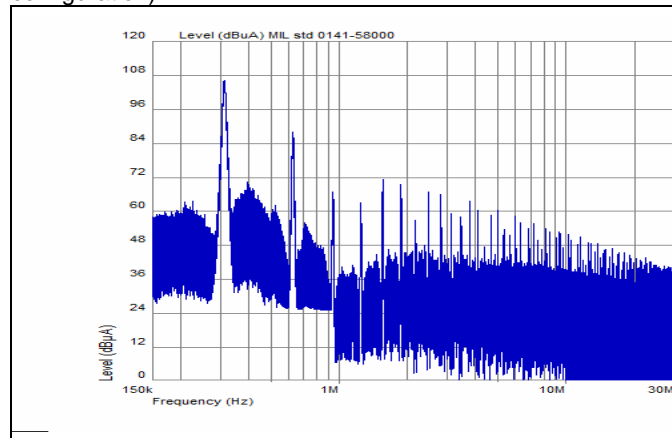
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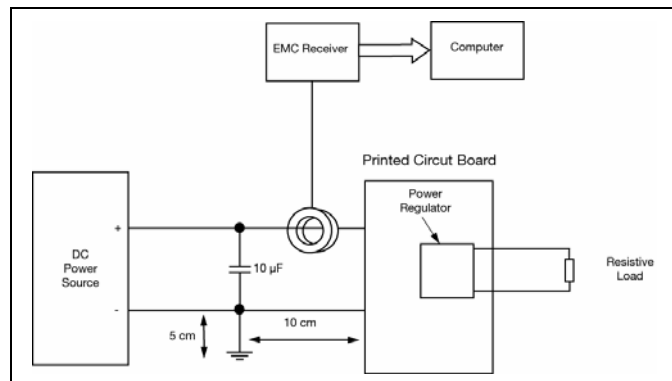
EMC Specification

Conducted EMI measured according to test set-up and standard MIL std 0141 - 58000.
The fundamental switching frequency is 320 kHz for BMR462 at $V_I = 12.0$ V, max I_O .

Conducted EMI Input terminal value (typical for default configuration)



EMI without filter



Test set-up

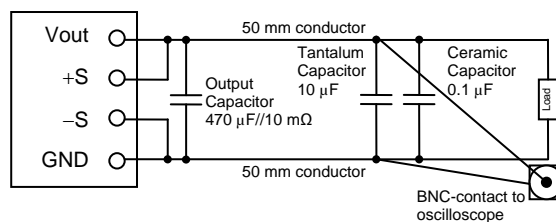
Layout Recommendations

The radiated EMI performance of the product will depend on the PWB layout and ground layer design. It is also important to consider the stand-off of the product. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis.

A ground layer will increase the stray capacitance in the PWB and improve the high frequency EMC performance.

Output Ripple and Noise

Output ripple and noise is measured according to figure below. A 50 mm conductor works as a small inductor forming together with the two capacitances a damped filter.



Output ripple and noise test set-up.

Operating information**Power Management Overview**

This product is equipped with a PMBus interface. The product incorporates a wide range of readable and configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults. A fault is also shown as an alert on the SALERT pin. The following product parameters can continuously be monitored by a host: Input voltage, output voltage/current, and internal temperature. If the monitoring is not needed it can be disabled and the product enters a low power mode reducing the power consumption. The protection features are not affected.

The product is delivered with a default configuration suitable for a wide range operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface. Please contact your local Ericsson Power Modules representative for design support of custom configurations or appropriate SW tools for design and down-load of your own configurations.

Input Voltage

The input voltage range, 4.5 - 14 V, makes the product easy to use in intermediate bus applications when powered by a non-regulated bus converter or a regulated bus converter. See Ordering Information for input voltage range.

Input Under Voltage Lockout, UVLO

The product monitors the input voltage and will turn-on and turn-off at configured levels. The default turn-on input voltage level setting is 4.20 V, whereas the corresponding turn-off input voltage level is 3.85 V. Hence, the default hysteresis between turn-on and turn-off input voltage is 0.35 V. Once an input turn-

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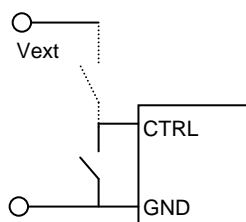
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off condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption. The unit will continue to operate as long as the input voltage can be supported. If the input voltage continues to fall, there will come a point where the unit will cease to operate.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.

The default response from a turn-off is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the product will be re-enabled. The turn-on and turn-off levels and response can be reconfigured using the PMBus interface.

Remote Control



The product is equipped with a remote control function, i.e., the CTRL pin. The remote control can be connected to either the primary negative input connection (GND) or an external voltage (Vext), which is a 3 - 5 V positive supply voltage in accordance to the SMBus Specification version 2.0.

The CTRL function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch. By default the product will turn on when the CTRL pin is left open and turn off when the CTRL pin is applied to GND. The CTRL pin has an internal pull-up resistor. When the CTRL pin is left open, the voltage generated on the CTRL pin is max 5.5 V. If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the CTRL pin.

The product can also be configured using the PMBus interface to be "Always on", or turn on/off can be performed with PMBus commands.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. The performance in some applications can be enhanced by addition of external capacitance as described under External Decoupling Capacitors. If the input voltage source contains significant inductance, the addition a capacitor with low ESR at the input of the product will ensure stable operation.

External Capacitors

Input capacitors:

The input ripple RMS current in a buck converter is equal to

$$\text{Eq. 1. } I_{\text{inputRMS}} = I_{\text{load}} \sqrt{D(1-D)},$$

where I_{load} is the output load current and D is the duty cycle.

The maximum load ripple current becomes $I_{\text{load}}/2$. The ripple current is divided into three parts, i.e., currents in the input source, external input capacitor, and internal input capacitor. How the current is divided depends on the impedance of the input source, ESR and capacitance values in the capacitors. A minimum capacitance of 300 μF with low ESR is recommended. The ripple current rating of the capacitors must follow Eq. 1. For high-performance/transient applications or wherever the input source performance is degraded, additional low ESR ceramic type capacitors at the input is recommended. The additional input low ESR capacitance above the minimum level insures an optimized performance.

Output capacitors:

When powering loads with significant dynamic current requirements, the voltage regulation at the point of load can be improved by addition of decoupling capacitors at the load. The most effective technique is to locate low ESR ceramic and electrolytic capacitors as close to the load as possible, using several capacitors in parallel to lower the effective ESR. The ceramic capacitors will handle high-frequency dynamic load changes while the electrolytic capacitors are used to handle low frequency dynamic load changes. Ceramic capacitors will also reduce high frequency noise at the load. It is equally important to use low resistance and low inductance PWB layouts and cabling.

External decoupling capacitors are a part of the control loop of the product and may affect the stability margins. Stable operation is guaranteed for the following total capacitance C_O in the output decoupling capacitor bank where

$$\text{Eq. 2. } C_O = [C_{\text{min}}, C_{\text{max}}] = [300, 7500] \mu\text{F}.$$

The decoupling capacitor bank should consist of capacitors which has a capacitance value larger than $C \geq C_{\text{min}}$ and has an ESR range of

$$\text{Eq. 3. } \text{ESR} = [\text{ESR}_{\text{min}}, \text{ESR}_{\text{max}}] = [5, 30] \text{ m}\Omega$$

The control loop stability margins are limited by the minimum time constant τ_{min} of the capacitors. Hence, the time constant of the capacitors should follow Eq. 4.

$$\text{Eq. 4. } \tau \geq \tau_{\text{min}} = C_{\text{min}} \text{ESR}_{\text{min}} = 1.5 \mu\text{s}$$

This relation can be used if your preferred capacitors have parameters outside the above stated ranges in Eq. 2 and Eq.3.

- If the capacitors capacitance value is $C < C_{\text{min}}$ one must use at least N capacitors where

$$N \geq \left\lceil \frac{C_{\text{min}}}{C} \right\rceil \text{ and } \text{ESR} \geq \text{ESR}_{\text{min}} \frac{C_{\text{min}}}{C}.$$

- If the ESR value is $\text{ESR} > \text{ESR}_{\text{max}}$ one must use at least N capacitors of that type where

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$$N \geq \left\lceil \frac{ESR}{ESR_{\max}} \right\rceil \text{ and } C \geq \frac{C_{\min}}{N}.$$

- If the ESR value is $ESR < ESR_{\min}$ the capacitance value should be

$$C \geq C_{\min} \frac{ESR_{\min}}{ESR}.$$

For a total capacitance outside the above stated range or capacitors that do not follow the stated above requirements above a re-design of the control loop parameters will be necessary for robust dynamic operation and stability.

Control Loop Compensation

The product is configured with a robust control loop compensation which allows for a wide range operation of input and output voltages and capacitive loads as defined in the section External Decoupling Capacitors. For an application with a specific input voltage, output voltage, and capacitive load, the control loop can be optimized for a robust and stable operation and with an improved load transient response. This optimization will minimize the amount of required output decoupling capacitors for a given load transient requirement yielding an optimized cost and minimized board space. The control loop parameters can be reconfigured using the PMBus interface.

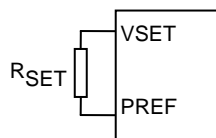
Load Transient Response Optimization

The product incorporates a Non-Linear transient Response, NLR, loop that decreases the response time and the output voltage deviation during a load transient. The NLR results in a higher equivalent loop bandwidth than is possible using a traditional linear control loop. The product is pre-configured with appropriate NLR settings for robust and stable operation for a wide range of input voltage and a capacitive load range as defined in the section External Decoupling Capacitors. For an application with a specific input voltage, output voltage, and capacitive load, the NLR configuration can be optimized for a robust and stable operation and with an improved load transient response. This will also reduce the amount of output decoupling capacitors and yield a reduced cost. However, the NLR reduces the efficiency. In order to obtain maximal energy efficiency the load transient requirement has to be met by the standard control loop compensation and the decoupling capacitors. The NLR settings can be reconfigured using the PMBus interface.

Remote Sense

The product has remote sense that can be used to compensate for voltage drops between the output and the point of load. The sense traces should be located close to the PWB ground layer to reduce noise susceptibility. Due to derating of internal output capacitance the voltage drop should be kept below $V_{DROPMAX} = (5.5 - V_{OUT}) / 2$. A large voltage drop will impact the electrical performance of the regulator. If the remote sense is not needed +S should be connected to VOUT and -S should be connected to GND.

Output Voltage Adjust using Pin-strap Resistor



Using an external Pin-strap resistor, R_{SET} , the output voltage can be set in the range 0.6 V to 5.5 V at 28 different levels shown in the table below. The resistor should be applied between the VSET pin and the PREF pin.

R_{SET} also sets the maximum output voltage, see section "Limiting the maximum output voltage". The resistor is sensed only during product start-up. Changing the resistor value during normal operation will not change the output voltage. The input voltage must be at least 1 V larger than the output voltage in order to deliver the correct output voltage. See Ordering Information for output voltage range.

The following table shows recommended resistor values for R_{SET} . Maximum 1% tolerance resistors are required.

V_{OUT} [V]	R_{SET} [kΩ]	V_{OUT} [V]	R_{SET} [kΩ]
0.60	10	1.50	46.4
0.65	11	1.60	51.1
0.70	12.1	1.70	56.2
0.75	13.3	1.80	61.9
0.80	14.7	1.90	68.1
0.85	16.2	2.00	75
0.90	17.8	2.10	82.5
0.95	19.6	2.20	90.9
1.00	21.5	2.30	100
1.05	23.7	2.50	110
1.10	26.1	3.00	121
1.15	28.7	3.30	133
1.20	31.6	4.00	147
1.25	34.8	5.00	162
1.30	38.3	5.50	178
1.40	42.2		

The output voltage and the maximum output voltage can be pin strapped to three fixed values by connecting the VSET pin according to the table below.

V_{OUT} [V]	VSET
0.60	Shorted to PREF
1.2	Open "high impedance"
2.5	Logic High, GND as reference

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Output Voltage Adjust using PMBus

The output voltage of the product can be configured using the PMBus interface in the range 0.54 to 5.5 V. See Ordering Information for output voltage range.

Maximum Output Voltage Protection

The output voltage range configurable by the PMBus interface is limited by the pin-strap resistor R_{SET} . R_{SET} sets the maximum output voltage to approximately 110% of the nominal output value, $V_{OUTMAX} = 1.1 \times V_{OUT} - calibration_offset$, where calibration offset is max 70 mV. A PMBus command can not set the output voltage higher than V_{OUTMAX} . This protects the load from an over voltage due to an accidental wrong PMBus command.

Over Voltage Protection (OVP)

The product includes over voltage limiting circuitry for protection of the load. The default OVP limit is 15% above the nominal output voltage. If the output voltage exceeds the OVP limit, the product can respond in different ways:

1. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side MOSFET and turn on the low-side MOSFET. The low-side MOSFET remains ON until the device attempts a restart, i.e. the output voltage is pulled to ground level (crowbar function).

The default response from an overvoltage fault is to immediately shut down as in 2. The device will continuously check for the presence of the fault condition, and when the fault condition no longer exists the device will be re-enabled. For continuous OVP when operating from an external clock for synchronization, the only allowed response is an immediate shutdown. The OVP limit and fault response can be reconfigured using the PMBus interface.

Under Voltage Protection (UVP)

The product includes output under voltage limiting circuitry for protection of the load. The default UVP limit is 15% below the nominal output voltage. The UVP limit can be reconfigured using the PMBus interface.

Power Good

The product provides a Power Good (PG) flag in the Status Word register that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. If specified in section Connections, the product also provides a PG pin. The PG pin is active high and by default open-drain but may also be configured as push-pull via the PMBus interface.

By default, the PG signal will be asserted if the output is within -10%/+15% of the target voltage. These limits may be changed via the PMBus interface. A PG delay period is defined as the time from when all conditions within the product for asserting PG are met to when the PG signal is actually asserted. By default, the PG delay is set equal to the soft-start ramp time

setting. Therefore, if the soft-start ramp time is set to 10 ms, the PG delay will be set to 10 ms. The PG delay may be set independently of the soft-start ramp using the PMBus interface.

Switching Frequency

The fundamental switching frequency is 320 kHz, which yields optimal power efficiency. The switching frequency can be set to any value between 200 kHz and 640 kHz using the PMBus interface. The switching frequency will change the efficiency/power dissipation, load transient response and output ripple. For optimal control loop performance the control loop must be re-designed when changing the switching frequency.

Synchronization

Synchronization is a feature that allows multiple products to be synchronized to a common frequency. Synchronized products powered from the same bus eliminate beat frequencies reflected back to the input supply, and also reduces EMI filtering requirements. Eliminating the slow beat frequencies (usually <10 kHz) allows the EMI filter to be designed to attenuate only the synchronization frequency. Synchronization can also be utilized for phase spreading, described in section Phase Spreading.

The products can be synchronized with an external oscillator or one product can be configured with the SYNC pin as a SYNC Output working as a master driving the synchronization. All others on the same synchronization bus should be configured with SYNC Input or SYNC Auto Detect (Default configuration) for correct operation. When the SYNC pin is configured in auto detect mode the product will automatically check for a clock signal on the SYNC pin.

Phase Spreading

When multiple products share a common DC input supply, spreading of the switching clock phase between the products can be utilized. This dramatically reduces input capacitance requirements and efficiency losses, since the peak current drawn from the input supply is effectively spread out over the whole switch period. This requires that the products are synchronized. Up to 16 different phases can be used. The phase spreading of the product can be configured using the PMBus interface.

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Adaptive Diode Emulation

Most power converters use synchronous rectification to optimize efficiency over a wide range of input and output conditions. However, at light loads the synchronous MOSFET will typically sink current and introduce additional energy losses associated with higher peak inductor currents, resulting in reduced efficiency. Adaptive diode emulation mode turns off the low-side FET gate drive at low load currents to prevent the inductor current from going negative, reducing the energy losses and increasing overall efficiency. Diode emulation is not available for current sharing groups. Note: the overall bandwidth of the product may be reduced when in diode emulation mode. It is recommended that diode emulation is disabled prior to applying significant load steps. The diode emulation mode can be configured using the PMBus interface.

Adaptive Frequency and Pulse Skip Control

Since switching losses contribute to the efficiency of the power converter, reducing the switching frequency will reduce the switching losses and increase efficiency. The product includes an Adaptive Frequency Control mode, which effectively reduces the observed switching frequency as the load decreases. Adaptive frequency mode is only available while the device is operating within Adaptive Diode Emulation Mode. As the load current is decreased, diode emulation mode decreases the Synch-FET on-time to prevent negative inductor current from flowing. As the load is decreased further, the Switch-FET pulse width will begin to decrease while maintaining the programmed frequency, f_{PROG} (set by the `FREQ_SWITCH` command). Once the Switch-FET pulse width (D) reaches 50% of the nominal duty cycle, D_{NOM} (determined by V_I and V_O), the switching frequency will start to decrease according to the following equation:

$$\text{Eq. 5. } f_{sw} = D \left(\frac{2(f_{PROG} - f_{MIN})}{D_{NOM}} \right) + f_{MIN}.$$

Disabling a minimum Synch-FET makes the product also pulse

skip which reduces the power loss further.

It should be noted that adaptive frequency mode is not available for current sharing groups and is not allowed when the device is placed in auto-detect mode and a clock source is present on the SYNC pin, or if the device is outputting a clock signal on its SYNC pin. The adaptive frequency and pulse skip modes can be configured using the PMBus interface.

Efficiency Optimized Dead Time Control

The product utilizes a closed loop algorithm to optimize the dead-time applied between the gate drive signals for the switch and synch FETs. The algorithm constantly adjusts the deadtime non-overlap to minimize the duty cycle, thus maximizing efficiency. This algorithm will null out deadtime differences due to component variation, temperature and loading effects. The algorithm can be configured via the PMBus interface.

Over Current Protection (OCP)

The product includes current limiting circuitry for protection at continuous overload. The following OCP response options are available:

3. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
4. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period
5. Continue operating for a given delay period, followed by shutdown if the fault still exists.
6. Continue operating through the fault (this could result in permanent damage to the product).
7. Initiate an immediate shutdown.

The default response from an over current fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition, and if the fault condition no longer exists the device will be re-enabled. The load distribution should be designed for the maximum output short circuit current specified. The OCP limit and response of the product can be reconfigured using the PMBus interface.

Start-up Procedure

The product follows a specific internal start-up procedure after power is applied to the VIN pin:

1. Status of the address and output voltage pin-strap pins are checked and values associated with the pin settings are loaded.
2. Values stored in the Ericsson default non-volatile memory are loaded. This overwrites any previously loaded values.
3. Values stored in the user non-volatile memory are loaded. This overwrites any previously loaded values.

Once this process is completed and the start-up time has passed (see Electrical Specification), the product is ready to be

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enabled using the CTRL pin. The product is also ready to accept commands via the PMBus interface, which will overwrite any values loaded during the start-up procedure.

Soft-start Power Up

The soft-start control introduces a time-delay before allowing the output voltage to rise. Once the start-up time has passed and the output has been enabled, the device requires approximately 2 ms before its output voltage may be allowed to start its ramp-up process. If a soft-start delay period less than 2 ms has been configured the device will default to a 2 ms delay period. If a delay period greater than 2 ms is configured, the device will wait for the configured delay period prior to starting to ramp its output. After the delay period has expired, the output will begin to ramp towards its target voltage according to the configured soft-start ramp time.

The default settings for the soft-start delay period and the soft-start ramp time is 10 ms. Hence, power-up is completed within 20 ms in default configuration using remote control. Precise timing reduces the delay time variations and is by default activated. The soft-start power up of the product can be reconfigured using the PMBus interface.

Output Voltage Sequencing

A group of products may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another. Multi-product sequencing can be achieved by configuring the start delay and rise time of each device through the PMBus interface and by using the CTRL start signal.

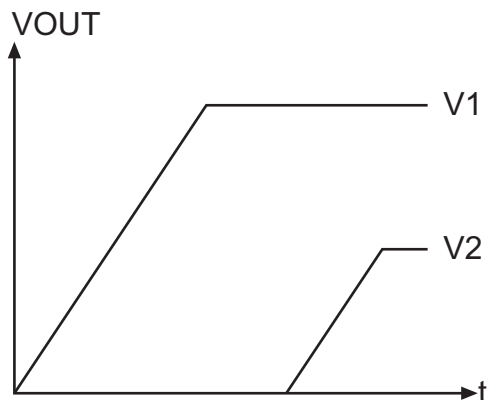


Illustration of Output Voltage Sequencing.

Voltage Tracking

The product integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. During ramp-up, the output voltage follows the VTRK voltage until the preset output voltage level is met. The product offers two modes of tracking as follows:

1. Coincident. This mode configures the product to ramp its output voltage at the same rate as the voltage applied to the VTRK pin.

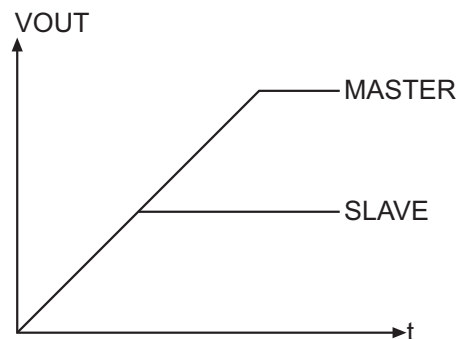


Illustration of Coincident Voltage Tracking.

2. Ratiometric. This mode configures the product to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but a different tracking ratio may be set by an external resistive voltage divider or through the PMBus interface.

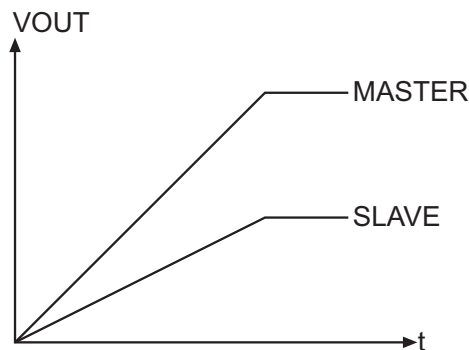


Illustration of Ratiometric Voltage Tracking

The master device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. All of the CTRL pins in the tracking group must be connected and driven by a single logic source. It should be noted that current sharing groups that are also configured to track another voltage do not offer pre-bias protection; a minimum load should therefore be enforced to avoid the output voltage from being held up by an outside force.

Voltage Margining Up/Down

The product can adjust its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. Margin limits of the nominal output voltage $\pm 5\%$ are default, but the margin limits can be reconfigured

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using the PMBus interface.

Pre-Bias Startup Capability

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual-supply logic component, such as FPGAs or ASICs. The BMR462 product family incorporates synchronous rectifiers, but will not sink current during startup, or turn off, or whenever a fault shuts down the product in a pre-bias condition. Pre-bias protection is not offered for current sharing groups that also have voltage tracking enabled.

Group Communication Bus

The Group Communication Bus, GCB, is used to communicate between products. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading, and current sharing. The GCB solves the PMBus data rate limitation. The GCB pin on all devices in an application should be connected together. For robust communication it is recommended that 27 ohm series resistors are placed, close to the GCB pin, between each device and the common GCB connection. A pull-up resistor is required on the common GCB in order to guarantee the rise time as follows:

$$\text{Eq. 6 } \tau = R_{GCB} C_{GCB} \leq 1\mu s,$$

where R_{GCB} is the pull up resistor value and C_{GCB} is the bus loading. The pull-up resistor should be tied to an external 3.3 V or 5 V supply voltage, which should be present prior to or during power-up.

Fault spreading

The product can be configured to broadcast a fault event over the GCB to the other devices in the group. When a non-destructive fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the GCB. The other devices on the GCB will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so.

Over Temperature Protection (OTP)

The products are protected from thermal overload by an internal over temperature shutdown circuit. When T_{P1} as defined in thermal consideration section exceeds 120°C the product will shut down. The product will make continuous attempts to start up and resume normal operation automatically when the temperature has dropped >15°C below the over temperature threshold. The specified OTP level and hysteresis are valid for worst case operation regarding convection, input voltage and output voltage. This means the OTP level and hysteresis in many cases will be lower. The OTP level, hysteresis, and fault response of the product can be reconfigured using the PMBus interface. The fault response can be configured as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts (default configuration).

2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

Optimization examples

This product is designed with a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. It is possible to change the configuration file to optimize certain performance characteristics. In the table below is a schematic view on how to change different configuration parameters in order to achieve an optimization towards a wanted performance.

↑	Increase
→	No change
↓	Decrease

Config. parameters	Switching frequency	Control loop bandwidth	NLR threshold	Diode emulation (DCM)	Min. pulse
Optimized performance					
Maximize efficiency	↓	→	↑	Enable	Disable
Minimize ripple ampl.	↑	→	↑	Enable or disable	Enable or disable
Improve load transient response	↑	↑	↓	Disable	Disable
Minimize idle power loss	↓	↑	→	Enable	Enable

P_{II}	Input idling power (no load)	Default configuration: Continues Conduction Mode, CCM	$V_O = 0.6 \text{ V}$	0.36	W
			$V_O = 1.0 \text{ V}$	0.35	
			$V_O = 3.3 \text{ V}$	0.54	
			$V_O = 5.0 \text{ V}$	0.97	
	DCM, Discontinues Conduction Mode		$V_O = 0.6 \text{ V}$	0.30	W
			$V_O = 1.0 \text{ V}$	0.37	
			$V_O = 3.3 \text{ V}$	0.41	

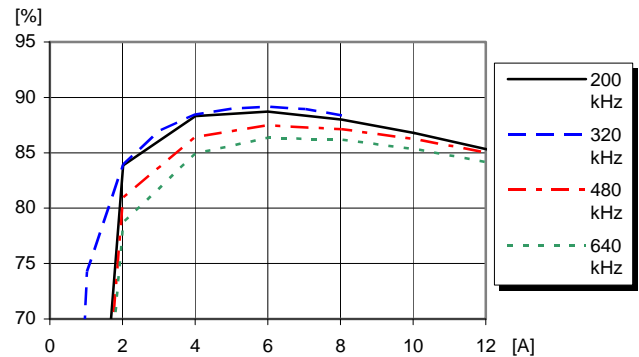
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Input 4.5-14 V, Output up to 12 A / 60 W

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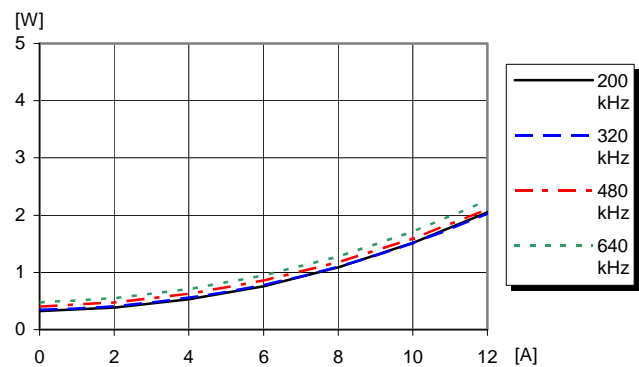
P_{ii}	Input idling power (no load)	DCM with Adaptive Frequency and Minimum Pulse Enabled	$V_O = 0.6 \text{ V}$	0.29	W
			$V_O = 1.0 \text{ V}$	0.35	
			$V_O = 3.3 \text{ V}$	0.37	
			$V_O = 5.0 \text{ V}$	0.42	
		DCM with Adaptive Frequency and Minimum Pulse Disabled	$V_O = 0.6 \text{ V}$	0.25	W
			$V_O = 1.0 \text{ V}$	0.20	
			$V_O = 3.3 \text{ V}$	0.20	
			$V_O = 5.0 \text{ V}$	0.20	
P_{CTRL}	Input standby power	Turned off with CTRL-pin	Default configuration: Monitoring enabled, Precise timing enabled	180	mW
			Monitoring enabled, Precise timing disabled	120	mW
			Low power mode: Monitoring disabled, Precise timing disabled	85	mW
V_{tr1}	Load transient peak voltage deviation	Default configuration $di/dt = 2 \text{ A}/\mu\text{s}$ $C_O = 470 \mu\text{F}$	$V_O = 0.6 \text{ V}$	55	mV
			$V_O = 1.0 \text{ V}$	65	
			$V_O = 3.3 \text{ V}$	110	
			$V_O = 5.0 \text{ V}$	190	
	Load step 25-75-25% of max I_O	Optimized PID and NLR configuration $di/dt = 2 \text{ A}/\mu\text{s}$ $C_O = 470 \mu\text{F}$	$V_O = 0.6 \text{ V}$	40	mV
			$V_O = 1.0 \text{ V}$	35	
			$V_O = 3.3 \text{ V}$	55	
			$V_O = 5.0 \text{ V}$	105	
t_{tr1}	Load transient recovery time	Default configuration $di/dt = 2 \text{ A}/\mu\text{s}$ $C_O = 470 \mu\text{F}$	$V_O = 0.6 \text{ V}$	230	us
			$V_O = 1.0 \text{ V}$	210	
			$V_O = 3.3 \text{ V}$	200	
			$V_O = 5.0 \text{ V}$	200	
	Load step 25-75-25% of max I_O	Optimized PID and NLR configuration $di/dt = 2 \text{ A}/\mu\text{s}$ $C_O = 470 \mu\text{F}$	$V_O = 0.6 \text{ V}$	45	
			$V_O = 1.0 \text{ V}$	40	
			$V_O = 3.3 \text{ V}$	40	
			$V_O = 5.0 \text{ V}$	35	

Efficiency vs. Output Current and Switching frequency



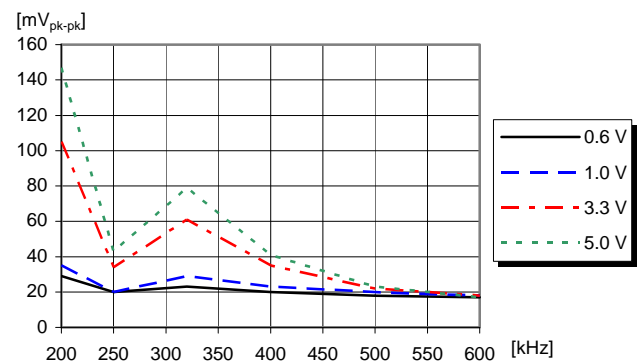
Efficiency vs. load current and switching frequency at $T_{P1} = +25^\circ\text{C}$, $V_I = 12 \text{ V}$, $V_O = 3.3 \text{ V}$, $C_O = 470 \mu\text{F}/10 \text{ m}\Omega$
Default configuration except changed frequency

Power Dissipation vs. Output Current and Switching frequency



Dissipated power vs. load current and switching frequency at $T_{P1} = +25^\circ\text{C}$, $V_I = 12 \text{ V}$, $V_O = 3.3 \text{ V}$, $C_O = 470 \mu\text{F}/10 \text{ m}\Omega$
Default configuration except changed frequency

Output Ripple vs. Switching frequency



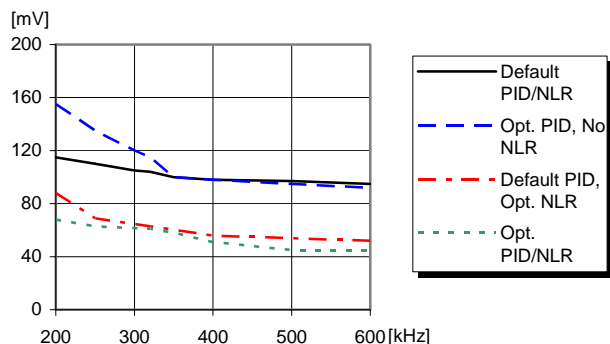
Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $V_I = 12 \text{ V}$, $C_O = 470 \mu\text{F}/10 \text{ m}\Omega$, $I_O = 12 \text{ A}$ resistive load. Default configuration except changed frequency.

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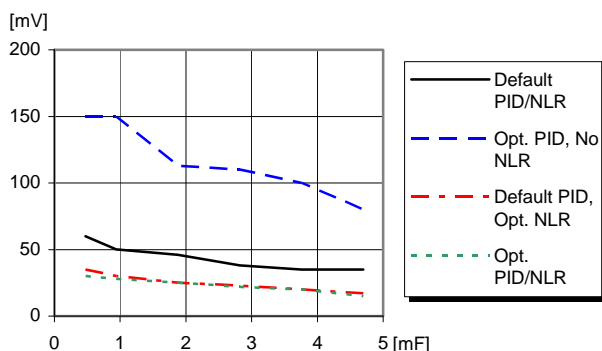
Load transient vs. Switching frequency



Load transient peak voltage deviation vs. frequency.
Step-change (3-9-3 A).

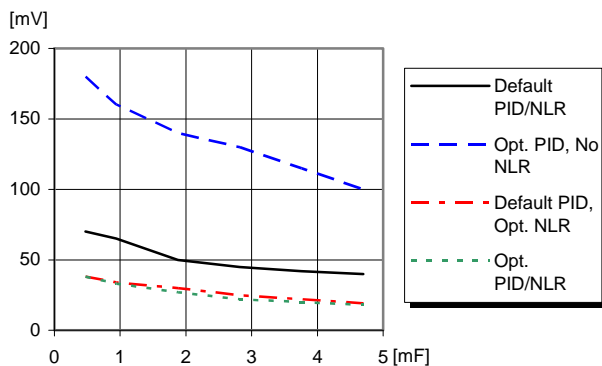
$T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$, $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$

Load Transient vs. Decoupling Capacitance, $V_O = 1.0\text{ V}$



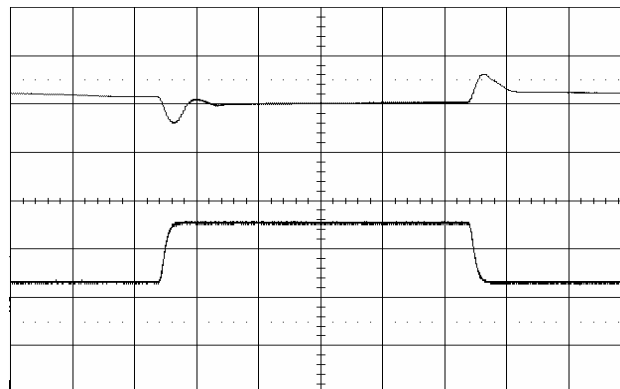
Load transient peak voltage deviation vs. decoupling capacitance.
Step-change (3-9-3 A). Parallel coupling of capacitors with $470\text{ }\mu\text{F}/10\text{ m}\Omega$,
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 1.0\text{ V}$, $f_{sw} = 320\text{ kHz}$, $di/dt = 2\text{ A}/\mu\text{s}$

Load Transient vs. Decoupling Capacitance, $V_O = 3.3\text{ V}$



Load transient peak voltage deviation vs. decoupling capacitance.
Step-change (3-9-3 A). Parallel coupling of capacitors with $470\text{ }\mu\text{F}/10\text{ m}\Omega$,
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$, $f_{sw} = 320\text{ kHz}$, $di/dt = 2\text{ A}/\mu\text{s}$

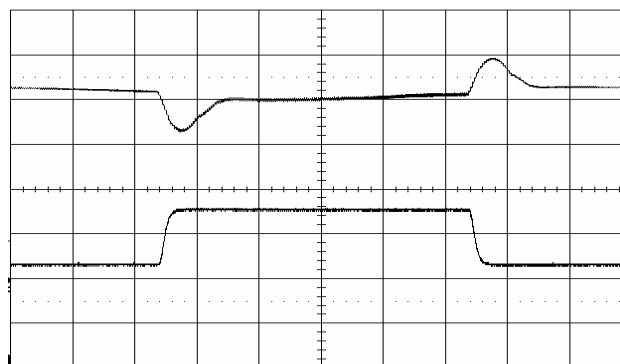
Output Load Transient Response, Default PID/NLR



Output voltage response to load current step-change (3-9-3 A) at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$
 $di/dt = 2\text{ A}/\mu\text{s}$, $f_{sw} = 320\text{ kHz}$, $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$
Default PID Control Loop and NLR

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

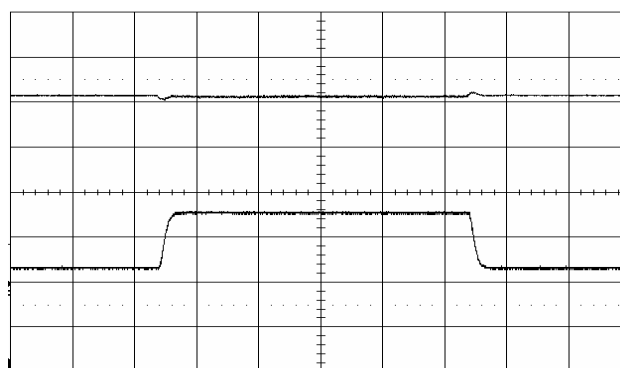
Output Load Transient Response, Optimized PID, no NLR



Output voltage response to load current step-change (3-9-3 A) at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$
 $di/dt = 2\text{ A}/\mu\text{s}$, $f_{sw} = 320\text{ kHz}$, $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$
Optimized PID Control Loop and no NLR

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

Output Load Transient Response, Optimized NLR



Output voltage response to load current step-change (3-9-3 A) at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$
 $di/dt = 2\text{ A}/\mu\text{s}$, $f_{sw} = 320\text{ kHz}$, $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$
Default PID Control Loop and optimized NLR

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

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Thermal Consideration

General

The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation. Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependant on the airflow across the product. Increased airflow enhances the cooling of the product. The Output Current Derating graph found in the Output section for each model provides the available output current vs. ambient air temperature and air velocity at specified V_I .

The product is tested on a 254 x 254 mm, 35 μ m (1 oz), test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm. The test board has 8 layers.

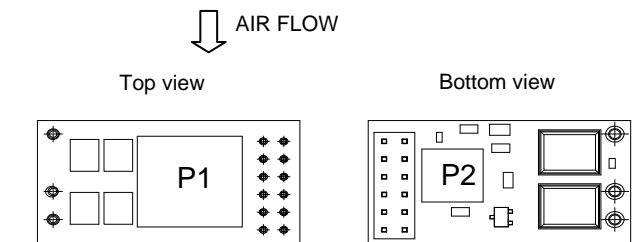
Proper cooling of the product can be verified by measuring the temperature at positions P1 and P2. The temperature at these positions should not exceed the max values provided in the table below. Note that the max value is the absolute maximum rating (non destruction) and that the electrical Output data is guaranteed up to $T_{P1} + 85^{\circ}\text{C}$.

See Design Note 019 for further information.

Definition of product operating temperature

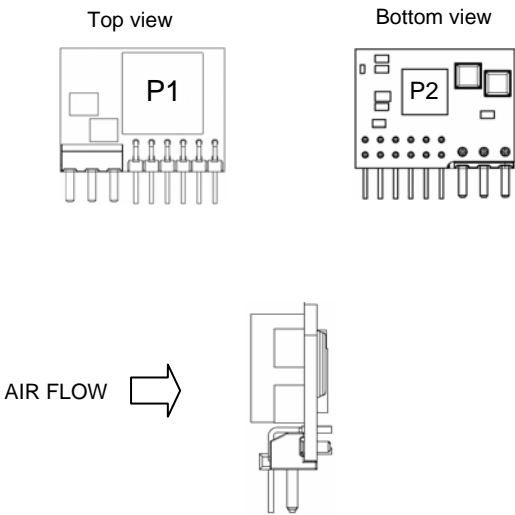
The product operating temperatures are used to monitor the temperature of the product, and proper thermal conditions can be verified by measuring the temperature at positions P1 and P2. The temperature at these positions (T_{P1} , T_{P2}) should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above maximum T_{P1} , measured at the reference point P1 are not allowed and may cause permanent damage.

Position	Description	Max Temp.
P1	Reference point, L1, inductor	120° C
P2	N1, control circuit	120° C



Temperature positions and air flow direction.

SIP version



Temperature positions and air flow direction.

Definition of reference temperature T_{P1}

The reference temperature is used to monitor the temperature limits of the product. Temperature above maximum T_{P1} , measured at the reference point P1 is not allowed and may cause degradation or permanent damage to the product. T_{P1} is also used to define the temperature range for normal operating conditions. T_{P1} is defined by the design and used to guarantee safety margins, proper operation and high reliability of the product.

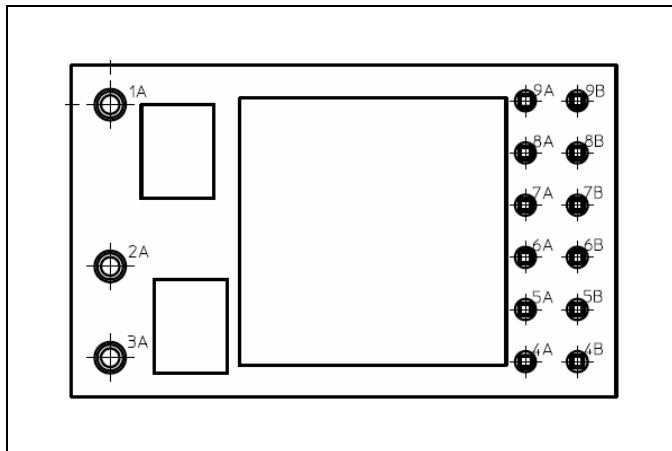
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Connections



Pin layout, top view (component placement for illustration only).

Pin	Designation	Function
1A	VIN	Input Voltage
2A	GND	Power Ground
3A	VOOUT	Output voltage
4A	VTRK	Voltage Tracking input
4B	SGND	Pin-strap Ground reference
5A	+S	Positive sense
5B	-S	Negative sense
6A	SA0	PMBus address pinstrap
6B	GCB	Group Communication Bus
7A	SCL	PMBus Clock
7B	SDA	PMBus Data
8A	VSET	Output voltage pinstrap
8B	SYNC	Synchronization I/O
9A	SALERT	PMBus Alert
9B	CTRL	PMBus Control (Remote Control)

PWB layout considerations

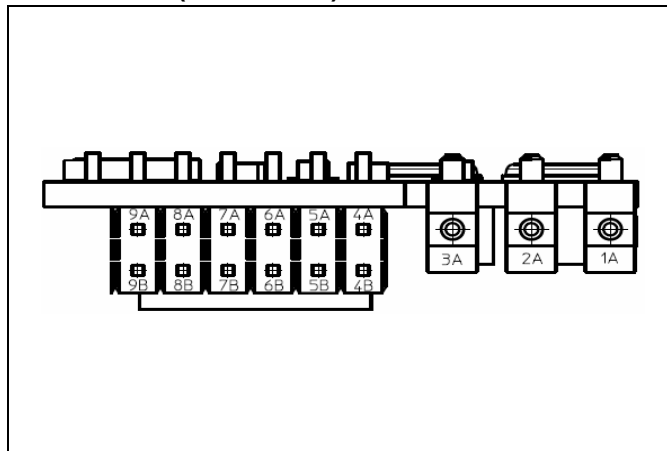
The pinstrap resistors, Rset, and R_{SA0} should be placed as close to the product as possible to minimize loops that may pick up noise.

Avoid current carrying planes under the pinstrap resistors and the PMBus signals.

The capacitor C_i (or capacitors implementing it) should be placed as close to the input pins as possible.

Capacitor C_o (or capacitors implementing it) should be placed close to the load.

Connections (SIP version)



Pin layout, side view (component placement for illustration only).

Pin	Designation	Function
1A	VIN	Input Voltage
2A	GND	Power Ground
3A	VOOUT	Output voltage
4A	+S	Positive sense
4B	-S	Negative sense
5A	VSET	Output voltage pin-strap
5B	VTRK	Voltage tracking input
6A	SALERT	PMBus Alert
6B	SDA	PMBus data
7A	SCL	PMBus Clock
7B	SYNC	Synchronization I/O
8A	SA0	PMBus address pin-strap
8B	CTRL	Remote Control
9A	GCB	Group Communication Bus
9B	PREF	Pin-strap Reference

Unused input pins

Unused SDA, SCL and GCB pins should still have pull-up resistors as specified. Unused VTRK or SYNC pins should be left unconnected or connected to the PREF pin. Unused CTRL pin can be left open due to internal pull-up.

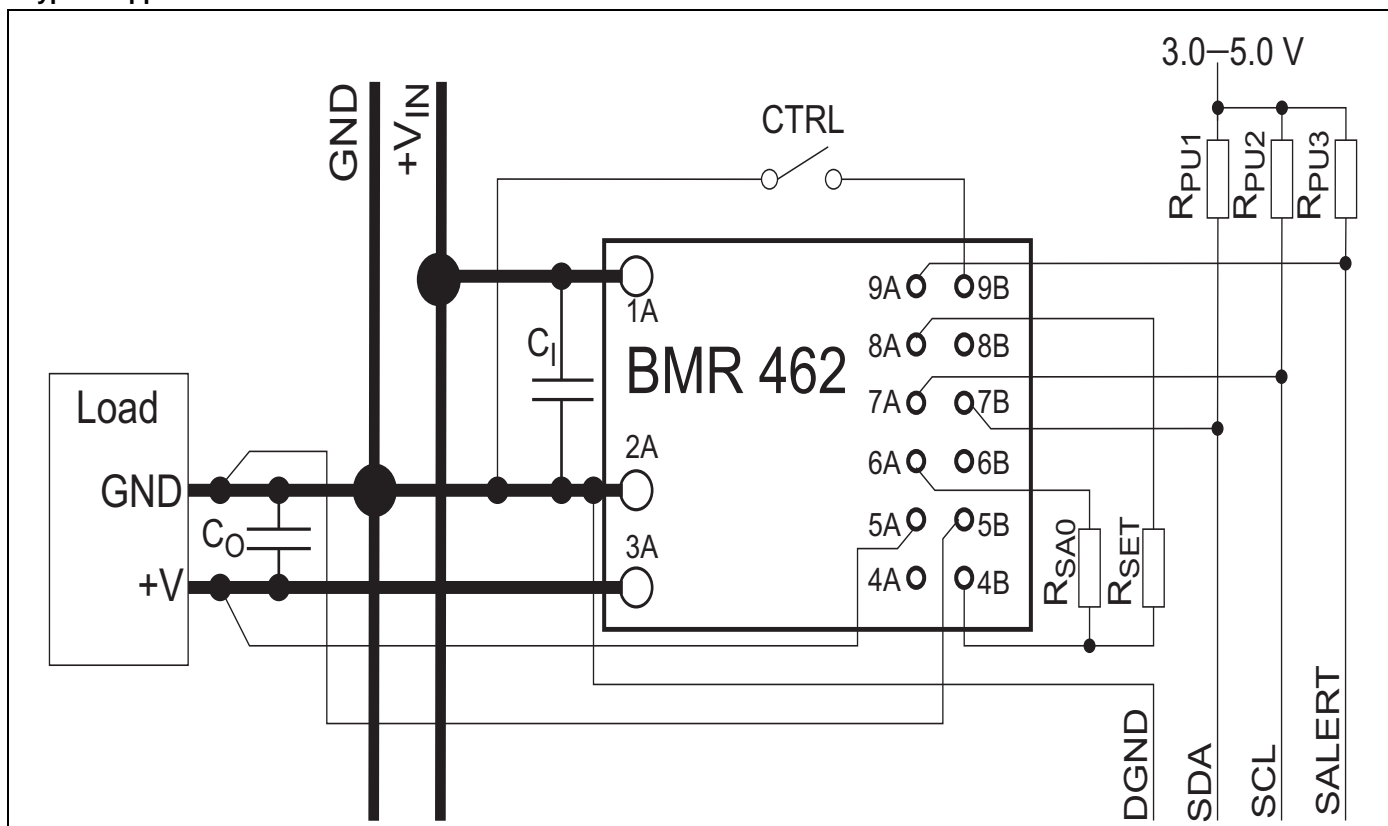
VSET and SA0/SA1 pins must have pinstrap resistors as specified.

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Typical Application Circuit



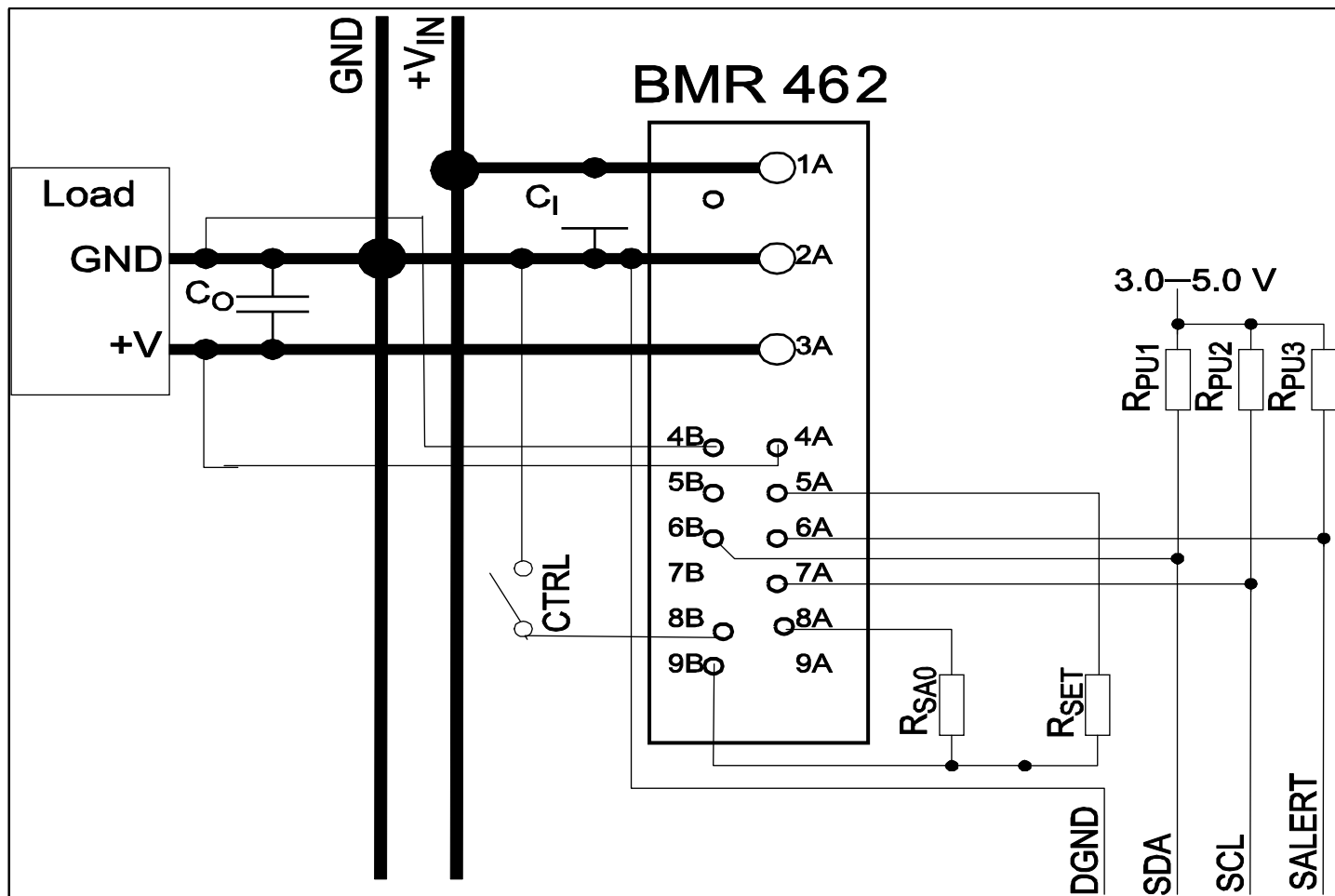
Standalone with PMBus communication

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Typical Application Circuit (SIP version)



Standalone with PMBus communication. Top side view of product footprint.

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PMBus Interface

This product provides a PMBus digital interface that enables the user to configure many aspects of the device operation as well as to monitor the input and output voltages, output current and device temperature. The product can be used with any standard two-wire I²C or SMBus host device. In addition, the module is compatible with PMBus version 1.1 and includes an SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring. The product supports 100 kHz bus clock frequency only. The PMBus signals, SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

$$\text{Eq. 7} \quad \tau = R_p C_p \leq 1\mu\text{s}$$

where R_p is the pull-up resistor value and C_p is the bus loading, the maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply voltage in range from 2.7 to 5.5V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.

Monitoring via PMBus

It is possible to monitor a wide variety of different parameters through the PMBus interface. Fault conditions can be monitored using the SALERT pin, which will be asserted when any number of pre-configured fault or warning conditions occur. It is also possible to continuously monitor one or more of the power conversion parameters including but not limited to the following:

- Input voltage
- Output voltage
- Output current
- Internal junction temperature
- Switching frequency
- Duty cycle

Snap Shot Parameter Capture

This product offers a special feature that enables the user to capture parametric data during normal operation or following a fault. The following parameters are stored:

- Input voltage
- Output voltage
- Output current
- Internal junction temperature
- Switching frequency
- Duty cycle
- Status registers

The Snapshot feature enables the user to read the parameters via the PMBus interface during normal operation, although it

should be noted that reading the 22 bytes will occupy the bus for some time. The Snapshot enables the user to store the snapshot parameters to Flash memory in response to a pending fault as well as to read the stored data from Flash memory after a fault has occurred. Automatic store to Flash memory following a fault is triggered when any fault threshold level is exceeded, provided that the specific fault response is to shut down. Writing to Flash memory is not allowed if the device is configured to restart following the specific fault condition. It should also be noted that the device supply voltage must be maintained during the time the device is writing data to Flash memory; a process that requires between 700-1400 μs depending on whether the data is set up for a block write. Undesirable results may be observed if the input voltage of the modules drops below 3.0 V during this process

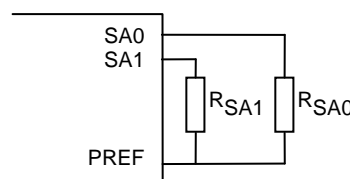
Software Tools for Design and Production

Ericsson provides software for configuration and monitoring of this product via the PMBus interface.

For more information please contact your local Ericsson sales representative.

PMBus Addressing

The PMBus address should be configured with resistors connected between the SA0/SA1 pins and the PREF pin, as shown in the figure below. Recommended resistor values for hard-wiring PMBus addresses are shown in the table. 1% tolerance resistors are required.



Schematic of connection of address resistor.

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Index	R _{SA} [kΩ]	Index	R _{SA} [kΩ]
0	10	13	34.8
1	11	14	38.3
2	12.1	15	42.2
3	13.3	16	46.4
4	14.7	17	51.1
5	16.2	18	56.2
6	17.8	19	61.9
7	19.6	20	68.1
8	21.5	21	75
9	23.7	22	82.5
10	26.1	23	90.9
11	28.7	24	100
12	31.6		

The PMBus address follows the equation below:

Eq. 8 PMBus Address (decimal) = 25 x (SA1 index) + (SA0 index)

The user can theoretically configure up to 625 unique PMBus addresses, however the PMBus address range is inherently limited to 128. Therefore, the user should use index values 0 - 4 on the SA1 pin and the full range of index values on the SA0 pin, which will provide 125 device address combinations. The user shall also be aware of further limitations of the address space as stated in the SMBus Specification.

Note that address 0x4B is allocated for production needs and can not be used.

Products with no SA1 pin have an internally defined SA1 index as follows.

Product	SA1 index
BMR 462	4

Optional PMBus Addressing

Alternatively the PMBus address can be defined by connecting the SA0/SA1 pins according to the following table. SA1 = open for products with no SA1 pin.

		SA0		
		low	open	high
SA1	low	0x20	0x21	0x22
	open	0x23	0x24	0x25
	high	0x26	0x27	Reserved

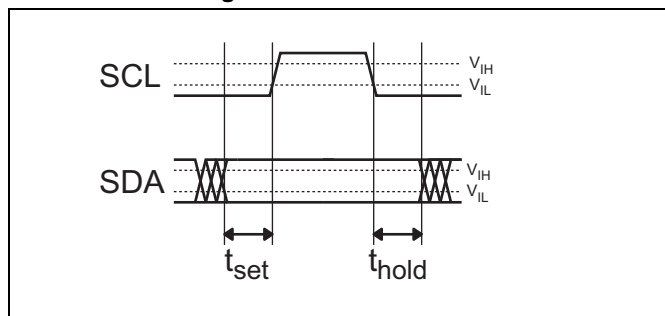
Low = Shorted to PREF

Open = High impedance

High = Logic high, GND as reference

Logic High definitions see Electrical Specification

I²C/SMBus – Timing



Setup and hold times timing diagram

The setup time, t_{set} , is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold} , is the time data, SDA, must be stable after the rising edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. When configuring the product, all standard SMBus protocols must be followed, including clock stretching. Additionally, a bus-free time delay between every SMBus transmission (between every stop & start condition) must occur. Refer to the SMBus specification, for SMBus electrical and timing requirements. Note that an additional delay of 20 ms has to be inserted in case of storing the RAM content into the internal non-volatile memory.

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PMBus Commands

The product is PMBus compliant. The following table lists the implemented PMBus commands. For more detailed information see PMBus Power System Management Protocol Specification; Part I – General Requirements, Transport and Electrical Interface and PMBus Power System Management Protocol; Part II – Command Language.

Designation	Cmd	Impl
Standard PMBus Commands		
Control Commands		
PAGE	00h	No
OPERATION	01h	Yes
ON_OFF_CONFIG	02h	Yes
WRITE_PROTECT	10h	No
Output Commands		
VOUT_MODE (Read Only)	20h	Yes
VOUT_COMMAND	21h	Yes
VOUT_TRIM	22h	Yes
VOUT_CAL_OFFSET	23h	Yes
VOUT_MAX	24h	Yes
VOUT_MARGIN_HIGH	25h	Yes
VOUT_MARGIN_LOW	26h	Yes
VOUT_TRANSITION_RATE	27h	Yes
VOUT_DROOP	28h	Yes
MAX_DUTY	32h	Yes
FREQUENCY_SWITCH	33h	Yes
IOUT_CAL_GAIN	38h	Yes
IOUT_CAL_OFFSET	39h	Yes
VOUT_SCALE_LOOP	29h	No
VOUT_SCALE_MONITOR	2Ah	No
COEFFICIENTS	30h	No
Fault Limit Commands		
POWER_GOOD_ON	5Eh	Yes
VOUT_OV_FAULT_LIMIT	40h	Yes
VOUT_UV_FAULT_LIMIT	44h	Yes
IOUT_OC_FAULT_LIMIT	46h	Yes
IOUT_UC_FAULT_LIMIT	4Bh	Yes
OT_FAULT_LIMIT	4Fh	Yes
OT_WARN_LIMIT	51h	Yes
UT_WARN_LIMIT	52h	Yes
UT_FAULT_LIMIT	53h	Yes
VIN_OV_FAULT_LIMIT	55h	Yes
VIN_OV_WARN_LIMIT	57h	Yes

Designation	Cmd	Impl
VIN_UV_WARN_LIMIT	58h	Yes
VIN_UV_FAULT_LIMIT	59h	Yes
VOUT_OV_WARN_LIMIT	42h	No
VOUT_UV_WARN_LIMIT	43h	No
IOUT_OC_WARN_LIMIT	4Ah	No
Fault Response Commands		
VOUT_OV_FAULT_RESPONSE	41h	Yes
VOUT_UV_FAULT_RESPONSE	45h	Yes
OT_FAULT_RESPONSE	50h	Yes
UT_FAULT_RESPONSE	54h	Yes
VIN_OV_FAULT_RESPONSE	56h	Yes
VIN_UV_FAULT_RESPONSE	5Ah	Yes
IOUT_OC_FAULT_RESPONSE	47h	No
IOUT_UC_FAULT_RESPONSE	4Ch	No
Time setting Commands		
TON_DELAY	60h	Yes
TON_RISE	61h	Yes
TOFF_DELAY	64h	Yes
TOFF_FALL	65h	Yes
TON_MAX_FAULT_LIMIT	62h	No
Status Commands (Read Only)		
CLEAR_FAULTS	03h	Yes
STATUS_BYTE	78h	Yes
STATUS_WORD	79h	Yes
STATUS_VOUT	7Ah	Yes
STATUS_IOUT	7Bh	Yes
STATUS_INPUT	7Ch	Yes
STATUS_TEMPERATURE	7Dh	Yes
STATUS_CML	7Eh	Yes
STATUS_MFR_SPECIFIC	80h	Yes
Monitor Commands (Read Only)		
READ_VIN	88h	Yes
READ_VOUT	8Bh	Yes
READ_IOUT	8Ch	Yes
READ_TEMPERATURE_1	8Dh	Yes
READ_TEMPERATURE_2	8Eh	No
READ_FAN_SPEED_1	90h	No
READ_DUTY_CYCLE	94h	Yes
READ_FREQUENCY	95h	Yes

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Designation	Cmd	Impl
Identification Commands (Read Only)		
PMBUS_REVISION	98h	Yes
MFR_ID	99h	Yes
MFR_MODEL	9Ah	Yes
MFR_REVISION	9Bh	Yes
MFR_LOCATION	9Ch	Yes
MFR_DATE	9Dh	Yes
MFR_SERIAL	9Eh	Yes
Group Commands		
INTERLEAVE	37h	Yes
Supervisory Commands		
STORE_DEFAULT_ALL	11h	Yes
RESTORE_DEFAULT_ALL	12h	Yes
STORE_USER_ALL	15h	Yes
RESTORE_USER_ALL	16h	Yes
Product Specific Commands		
Time Setting Commands		
POWER_GOOD_DELAY	D4h	Yes
Fault limit Commands		
IOUT_AVG_OC_FAULT_LIMIT	E7h	Yes
IOUT_AVG_UC_FAULT_LIMIT	E8h	Yes
Fault Response Commands		
MFR_IOUT_OC_FAULT_RESPONSE	E5h	Yes
MFR_IOUT_UC_FAULT_RESPONSE	E6h	Yes
OVUV_CONFIG	D8h	Yes
Configuration and Control Commands		
MFR_CONFIG	D0h	Yes
USER_CONFIG	D1h	Yes
MISC_CONFIG	E9h	Yes
PID_TAPS	D5h	Yes
INDUCTOR	D6h	Yes
NLR_CONFIG	D7h	Yes
TEMPCO_CONFIG	DCh	Yes
DEADTIME	DDh	Yes
DEADTIME_CONFIG	DEh	Yes
DEADTIME_MAX	BFh	Yes
SNAPSHOT	EAh	Yes
SNAPSHOT_CONTROL	F3h	Yes
DEVICE_ID	E4h	Yes
USER_DATA_00	B0h	Yes

Designation	Cmd	Impl
Group Commands		
SEQUENCE	E0h	Yes
GCB_GROUP	E2h	Yes
ISHARE_CONFIG	D2h	Yes
PHASE_CONTROL	F0h	Yes
Supervisory Commands		
PRIVATE_PASSWORD	FBh	Yes
PUBLIC_PASSWORD	FCh	Yes
UNPROTECT	FDh	Yes
SECURITY_LEVEL	FAh	Yes

Notes:

Cmd is short for Command.

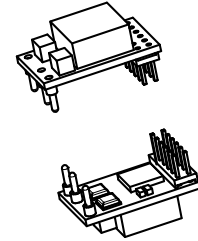
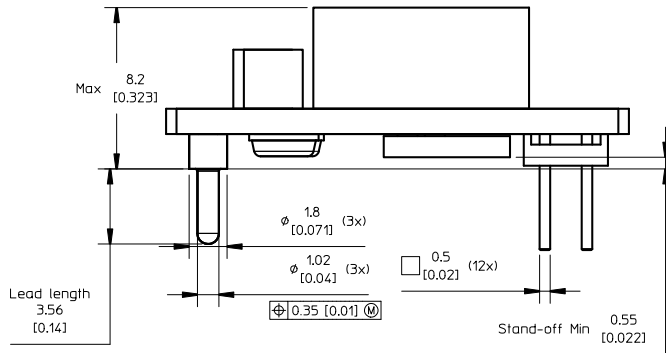
Impl is short for Implemented.

BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

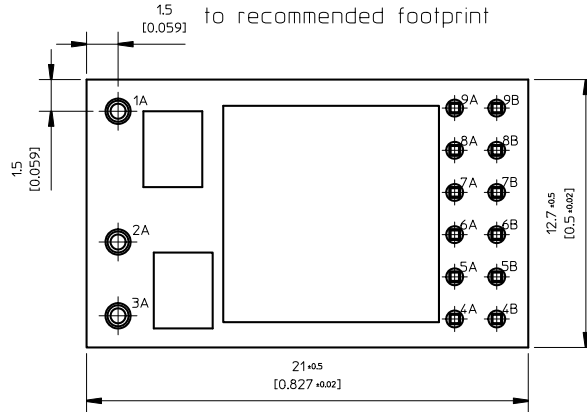
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Mechanical Information - Hole Mount, Open Frame Version



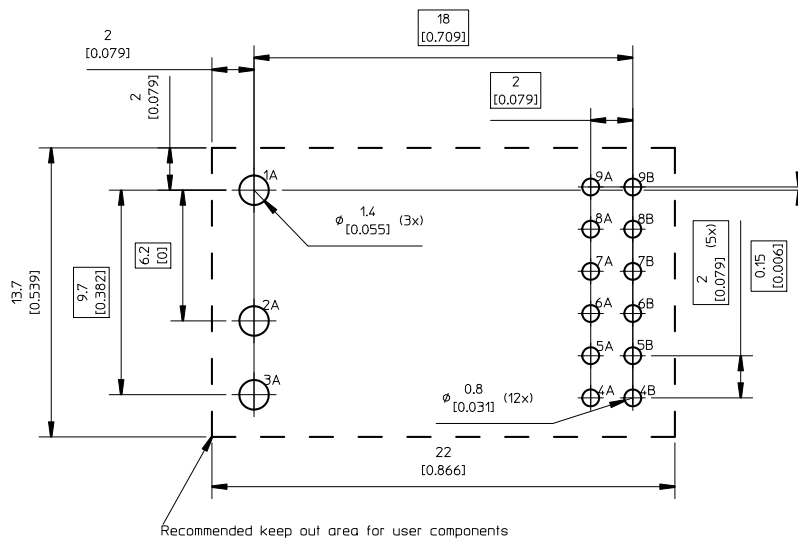
TOP VIEW
Pin positions according
to recommended footprint



PIN SPECIFICATIONS

Pin 1A-3A Material: Copper alloy
Plating: Min Matte tin 8-13 μm over 2.5-5 μm Ni.
Pin 4A-9B Material: Brass
Plating: Min Au 0.2 μm over 1.27 μm Ni.

RECOMMENDED FOOTPRINT - TOP VIEW



Weight: Typical 5 g
All dimensions in mm [inch]
Tolerances unless specified:
x.x ± 0.5 mm [0.02]
x.xx ± 0.25 mm [0.01]
(not applied on footprint or typical values)

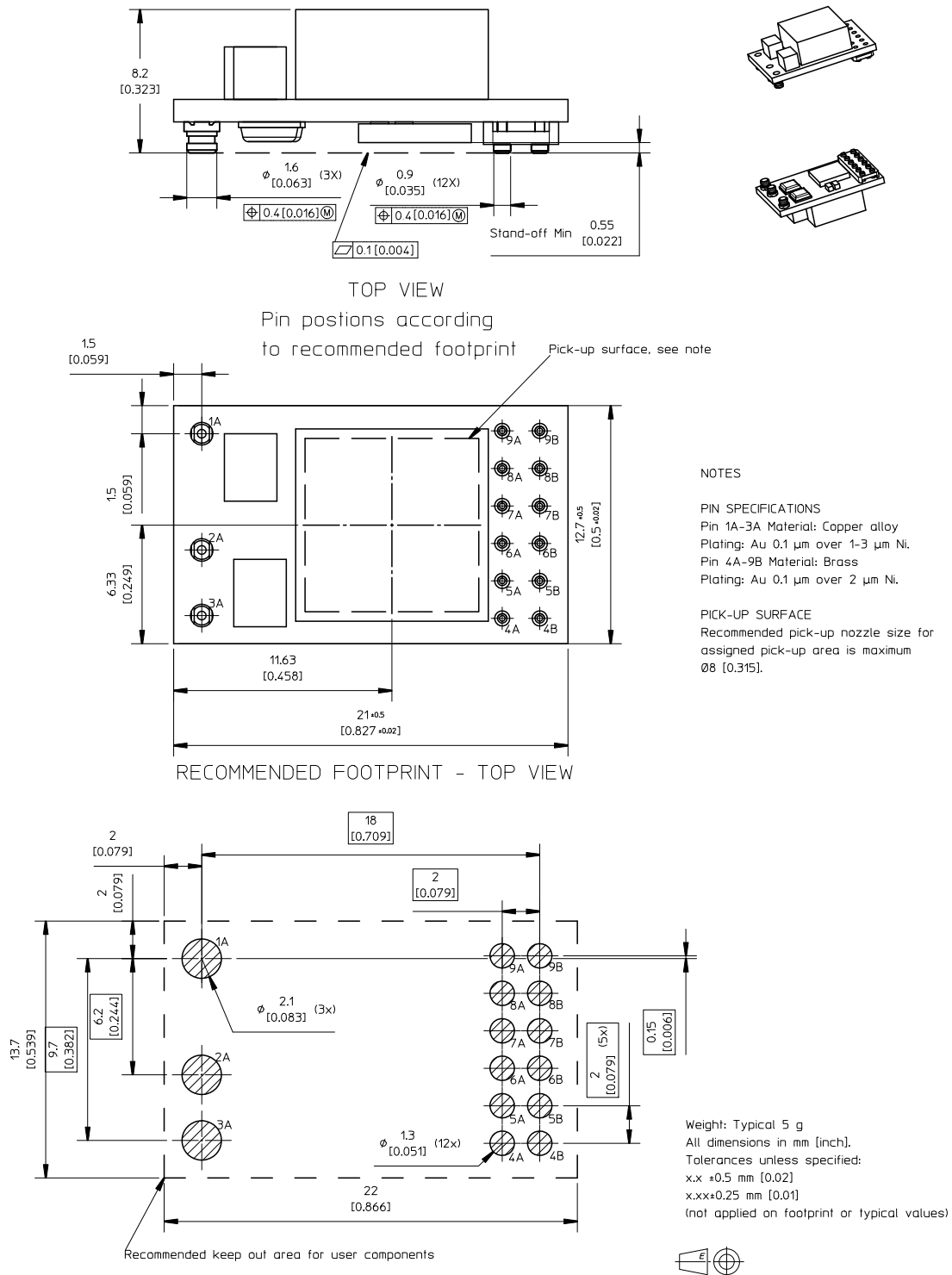


BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

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Mechanical Information - Surface Mount Version



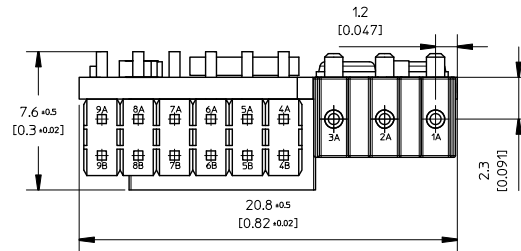
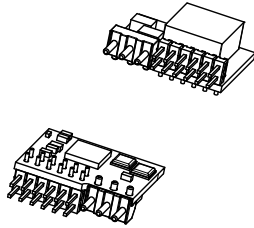
Technical Specification

BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

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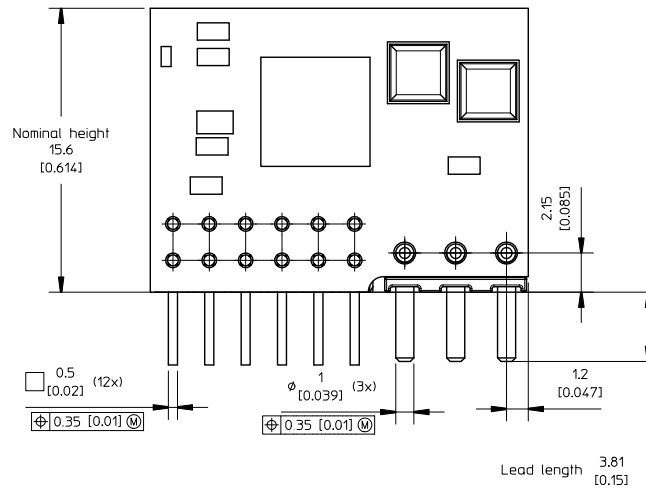
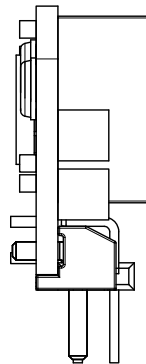
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Mechanical Information - Hole Mount, Open Frame Version (SIP version)



TOP VIEW

Pin positions according
to recommended footprint

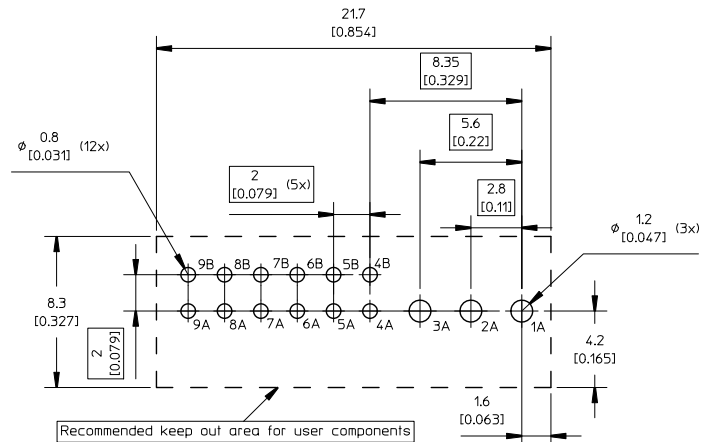


RECOMMENDED FOOTPRINT - TOP VIEW

PIN SPECIFICATIONS

Pin 1A-3A Material: Brass
 Plating: Min Au 0.1 µm Au over 1-3 µm Ni.
 Pin 4A-9B Material: Brass
 Plating: Min Au 0.1 µm over 1 µm Ni.

Weight: Typical 5.1 g
 All dimensions in mm [inch]
 Tolerances unless specified:
 x.x ±0.50 [0.02]
 x.x.x±0.25 [0.01]
 (not applied on footprint or typical values)



BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

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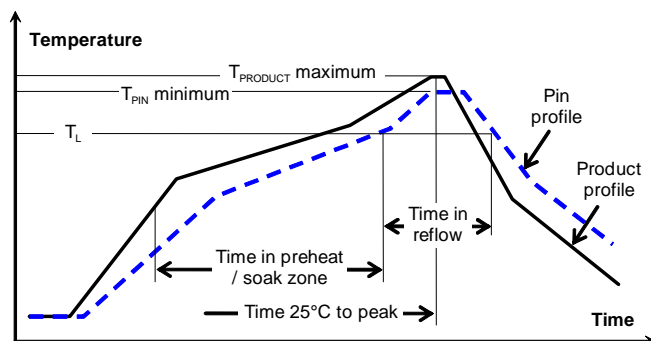
Soldering Information - Surface Mounting

The surface mount product is intended for forced convection or vapor phase reflow soldering in SnPb or Pb-free processes.

The reflow profile should be optimised to avoid excessive heating of the product. It is recommended to have a sufficiently extended preheat time to ensure an even temperature across the host PCB and it is also recommended to minimize the time in reflow.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long time reliability and isolation voltage.

General reflow process specifications		SnPb eutectic	Pb-free
Average ramp-up (T_{PRODUCT})		3°C/s max	3°C/s max
Typical solder melting (liquidus) temperature	T_L	183°C	221°C
Minimum reflow time above T_L		30 s	30 s
Minimum pin temperature	T_{PIN}	210°C	235°C
Peak product temperature	T_{PRODUCT}	225°C	260°C
Average ramp-down (T_{PRODUCT})		6°C/s max	6°C/s max
Maximum time 25°C to peak		6 minutes	8 minutes



Minimum Pin Temperature Recommendations

Pin number 2A chosen as reference location for the minimum pin temperature recommendation since this will likely be the coolest solder joint during the reflow process.

SnPb solder processes

For SnPb solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature, (T_L , 183°C for Sn63Pb37) for more than 30 seconds and a peak temperature of 210°C is recommended to ensure a reliable solder joint.

For dry packed products only: depending on the type of solder paste and flux system used on the host board, up to a recommended maximum temperature of 245°C could be used, if the products are kept in a controlled environment (dry pack handling and storage) prior to assembly.

Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature (T_L , 217 to 221°C for SnAgCu solder alloys) for more than 30 seconds and a peak temperature of 235°C on all solder joints is recommended to ensure a reliable solder joint.

Maximum Product Temperature Requirements

Top of the product PCB near pin 9B is chosen as reference location for the maximum (peak) allowed product temperature (T_{PRODUCT}) since this will likely be the warmest part of the product during the reflow process.

SnPb solder processes

For SnPb solder processes, the product is qualified for MSL 1 according to IPC/JEDEC standard J-STD-020C.

During reflow T_{PRODUCT} must not exceed 225 °C at any time.

Pb-free solder processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C.

During reflow T_{PRODUCT} must not exceed 260 °C at any time.

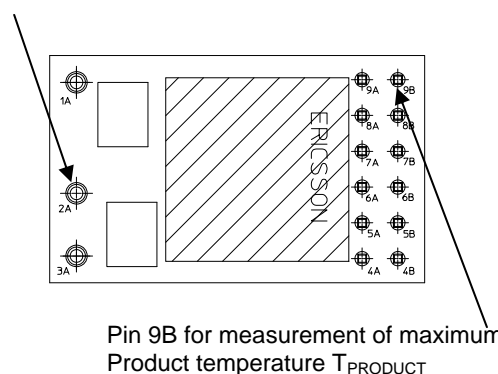
Dry Pack Information

Surface mounted versions of the products are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033 (Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices).

Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J-STD-033.

Thermocouple Attachment

Pin 2A for measurement of minimum Pin (solder joint) temperature T_{PIN}



Technical Specification

BMR 462 series POL Regulators
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Soldering Information - Hole Mounting

The hole mounted product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds.

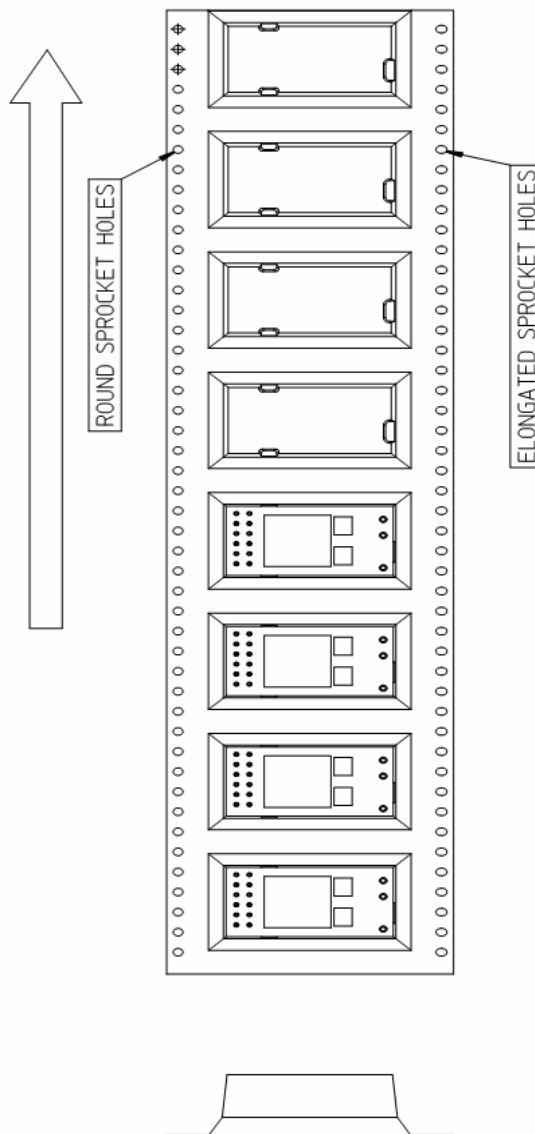
A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

Delivery Package Information

The products are delivered in antistatic carrier tape (EIA 481 standard).

Carrier Tape Specifications	
Material	PS, antistatic
Surface resistance	< 10 ⁷ Ohm/square
Bakeability	The tape is not bakable
Tape width, W	44 mm [1.73 inch]
Pocket pitch, P_t	24 mm [0.95 inch]
Pocket depth, K₀	12.3 mm [0.488 inch]
Reel diameter	381 mm [15 inch]
Reel capacity	200 products /reel
Reel weight	1290 g/full reel



Technical Specification

BMR 462 series POL Regulators
Input 4.5-14 V, Output up to 12 A / 60 W

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Soldering Information - Hole Mounting (SIP version)

The hole mounted product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds.

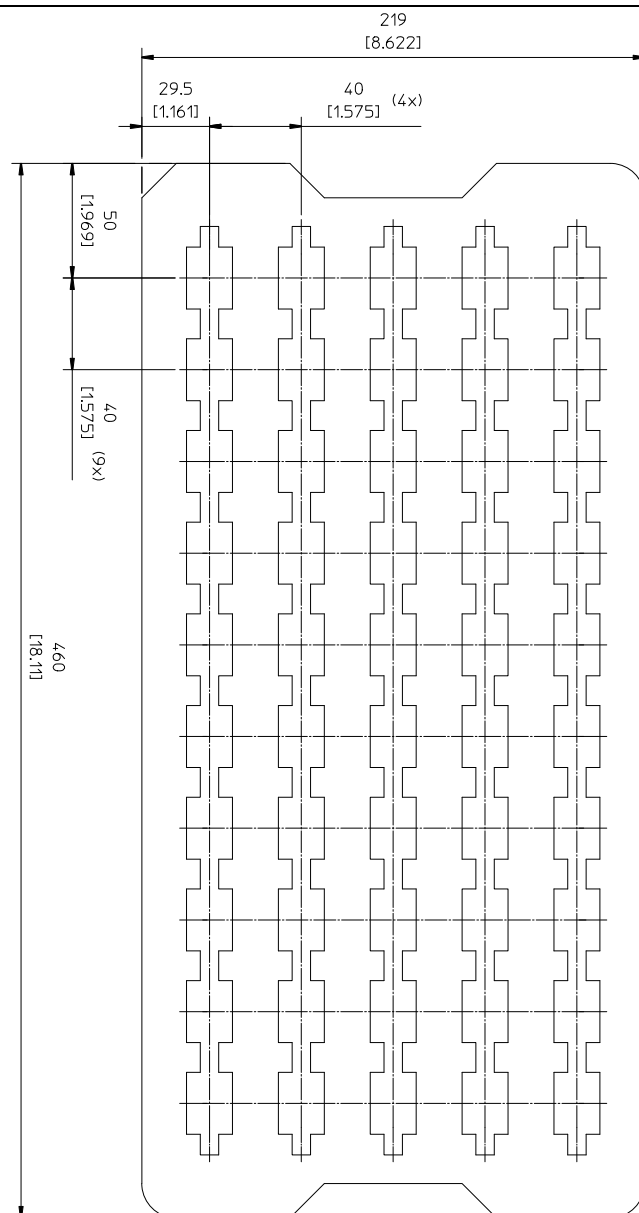
A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

Delivery Package Information (SIP version)

The products are delivered in antistatic/static dissipative trays

Tray Specifications	
Material	Antistatic Polyethylene foam
Surface resistance	1e5-1e12 Ohms/square
Bakability	The trays are not bakeable
Tray thickness	15 mm [0.591 inch]
Box capacity	100 products, 2 full trays/box)
Tray weight	35 g empty tray, 290 g full tray



Technical Specification

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Product Qualification Specification

Characteristics			
External visual inspection	IPC-A-610		
Change of temperature (Temperature cycling)	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 100°C 1000 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature T _A Duration	-45°C 72 h
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85 % RH 1000 hours
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 h
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Glycol ether	55°C 35°C
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Moisture reflow sensitivity ¹	J-STD-020C	Level 1 (SnPb-eutectic) Level 3 (Pb Free)	225°C 260°C
Operational life test	MIL-STD-202G, method 108A	Duration	1000 h
Resistance to soldering heat ²	IEC 60068-2-20 Tb, method 1A	Solder temperature Duration	270°C 10-13 s
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability	IEC 60068-2-58 test Td ¹	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	150°C dry bake 16 h 215°C 235°C
	IEC 60068-2-20 test Ta ²	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	Steam ageing 235°C 245°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g ² /Hz 10 min in each direction

Notes

¹ Only for products intended for reflow soldering (surface mount products)

² Only for products intended for wave soldering (plated through hole products)

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Key Features

- Small package
25.65 x 13.8 x 8.2 mm (1.01 x 0.543 x 0.323 in)
SIP: 26.3 x 7.6 x 15.6 mm (1.035 x 0.30 x 0.614 in)
- 0.6 V - 3.3 V output voltage range
- High efficiency, typ. 97.1% at 5Vin, 3.3Vout half load
- Configuration and Monitoring via PMBus
- Synchronization & phase spreading
- Current sharing, Voltage Tracking & Voltage margining
- MTBF 20 Mh

General Characteristics

- Fully regulated
- For narrow board pitch applications (15 mm/0.6 in)
- Non-Linear Response for reduction of decoupling cap.
- Input under voltage shutdown
- Over temperature protection
- Output short-circuit & Output over voltage protection
- Remote Control & Power Good
- Voltage setting via pin-strap or PMBus
- Advanced Configurable via Graphical Used Interface
- ISO 9001/14001 certified supplier
- Highly automated manufacturing ensures quality



Safety Approvals



Design for Environment



Meets requirements in high-temperature lead-free soldering processes.

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Technical Specification

BMR 463 series POL Regulators
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Ordering Information

Product program	Output
BMR 463	0.6-3.3 V, 20 A/ 66 W

Product number and Packaging

BMR 463 n ₁ n ₂ n ₃ n ₄ /n ₅ n ₆ n ₇ n ₈									
Options	n ₁	n ₂	n ₃	n ₄	/	n ₅	n ₆	n ₇	n ₈
Mounting	o				/				
Mechanical		o			/				
Interface			o	o	/				
Configuration					/	o	o	o	
Packaging					/				o

Options	Description
n ₁	0 Through hole mount version (TH) 1 Surface mount version (SMD) 2 Single in line (SIP)
n ₂	0 Open frame
n ₃ n ₄	02 PMBus and analog pin strap
n ₅ n ₆ n ₇	001 Standard configuration
n ₈	B Antistatic tray of 100 products (SIP only) C Antistatic tape & reel of 200 products (Sample delivery available in lower quantities. Not for SIP)

Example: A through-hole mounted, open frame, PMBus and analog pin strap, basic configuration with antistatic tape & reel packaging would be BMR 463 0002/001C

General Information

Reliability

The failure rate (λ) and mean time between failures (MTBF) is calculated at max output power and an operating ambient temperature (T_A) of +40°C. Different calculations methods could be used which may give different results. Ericsson Power Modules uses Telcordia SR-332 Issue 2 Method 1 (parts count method) to calculate the mean steady-state failure rate and standard deviation (σ). MTBF = $1/\lambda$.

MTBF for the BMR 463 series = 20 Mh and σ = 12 Mh

Telcordia SR-332 Issue 2 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

MTBF at 90% confidence level = 15 Mh

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2002/95/EC and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Ericsson Power Modules products include:

- Lead in glass of electronics components [5]
- Lead as an alloying element in copper alloy containing up to 4% lead by weight [6 c]
- Lead in high melting temperature type solder [7a]
- Lead in electronic ceramic parts [7c]
- Lead in solders to complete a viable connection between semiconductor die and carrier within integrated circuit flip chip packages [15]

Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of our products.

Warranty

Warranty period and conditions are defined in Ericsson Power Modules General Terms and Conditions of Sale.

Limitation of Liability

Ericsson Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

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Input 4.5-14 V, Output up to 20 A / 66 W

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Safety Specification**General information**

Ericsson Power Modules DC/DC converters and DC/DC regulators are designed in accordance with safety standards IEC/EN/UL 60950-1 *Safety of Information Technology Equipment*.

IEC/EN/UL 60950-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Energy hazards
- Fire
- Mechanical and heat hazards
- Radiation hazards
- Chemical hazards

On-board DC/DC converters and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without "Conditions of Acceptability". Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use should comply with the requirements in IEC 60950-1, EN 60950-1 and UL 60950-1 *Safety of Information Technology Equipment*. There are other more product related standards, e.g. IEEE 802.3 CSMA/CD (Ethernet) Access Method, and ETS-300132-2 *Power supply interface at the input to telecommunications equipment, operated by direct current (dc)*, but all of these standards are based on IEC/EN/UL 60950-1 with regards to safety.

Ericsson Power Modules DC/DC converters and DC/DC regulators are UL 60950-1 recognized and certified in accordance with EN 60950-1.

The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

The products should be installed in the end-use equipment, in accordance with the requirements of the ultimate application. Normally the output of the DC/DC converter is considered as SELV (Safety Extra Low Voltage) and the input source must be isolated by minimum Double or Reinforced Insulation from the primary circuit (AC mains) in accordance with IEC/EN/UL 60950-1.

Isolated DC/DC converters

It is recommended that a slow blow fuse is to be used at the input of each DC/DC converter. If an input filter is used in the circuit the fuse should be placed in front of the input filter.

In the rare event of a component problem that imposes a short circuit on the input source, this fuse will provide the following functions:

- Isolate the fault from the input power source so as not to affect the operation of other parts of the system.
- Protect the distribution wiring from excessive current and power loss thus preventing hazardous overheating.

The galvanic isolation is verified in an electric strength test. The test voltage (V_{iso}) between input and output is 1500 Vdc or 2250 Vdc (refer to product specification).

24 V DC systems

The input voltage to the DC/DC converter is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

48 and 60 V DC systems

If the input voltage to the DC/DC converter is 75 Vdc or less, then the output remains SELV (Safety Extra Low Voltage) under normal and abnormal operating conditions.

Single fault testing in the input power supply circuit should be performed with the DC/DC converter connected to demonstrate that the input voltage does not exceed 75 Vdc.

If the input power source circuit is a DC power system, the source may be treated as a TNV-2 circuit and testing has demonstrated compliance with SELV limits in accordance with IEC/EN/UL60950-1.

Non-isolated DC/DC regulators

The input voltage to the DC/DC regulator is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

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Input 4.5-14 V, Output up to 20 A / 66 W

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Electrical Specification
BMR 463 0002, BMR 463 1002
 $T_{P1} = -30$ to $+95^{\circ}\text{C}$, $V_I = 4.5$ to 14 V, $V_I > V_O + 1.0$ V

Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12.0$ V, max I_O , unless otherwise specified under Conditions.

Default configuration file, 190 10-CDA 102 0175/001.

External $C_{IN} = 470$ $\mu\text{F}/10$ m Ω , $C_{OUT} = 470$ $\mu\text{F}/10$ m Ω . See Operating Information section for selection of capacitor types.

Sense pins are connected to the output pins.

Characteristics	Conditions	min	typ	max	Unit
V_I	Input voltage rise time			2.4	V/ms

V_O	Output voltage without pin strap		1.2		V
	Output voltage adjustment range	0.60		3.3	V
	Output voltage adjustment including margining	0.54		3.63	V
	Output voltage set-point resolution		± 0.025		% V_O
	Output voltage accuracy	Includes, line, load, temp.	-1	1	%
	Line regulation	$V_O = 0.6$ V	2		mV
		$V_O = 1.0$ V	2		
		$V_O = 1.8$ V	2		
		$V_O = 3.3$ V	3		
	Load regulation; $I_O = 0 - 100\%$	$V_O = 0.6$ V	3		mV
		$V_O = 1.0$ V	2		
		$V_O = 1.8$ V	2		
		$V_O = 3.3$ V	2		
V_{Oac}	Output ripple & noise $C_O = 470$ μF (minimum external capacitance). See Note 12	$V_O = 0.6$ V	20		mVp-p
		$V_O = 1.0$ V	30		
		$V_O = 1.8$ V	40		
		$V_O = 3.3$ V	60		

I_O	Output current		20	A
I_S	Static input current at max I_O	$V_O = 0.6$ V	1.26	A
		$V_O = 1.0$ V	1.94	
		$V_O = 1.8$ V	3.31	
		$V_O = 3.3$ V	5.89	
I_{lim}	Current limit threshold	22	30	A
I_{sc}	Short circuit current	RMS, hiccup mode, See Note 3	$V_O = 0.6$ V	A
			$V_O = 1.0$ V	
			$V_O = 1.8$ V	
			$V_O = 3.3$ V	

η	Efficiency	50% of max I_O	$V_O = 0.6$ V	84.0	%
			$V_O = 1.0$ V	89.3	
			$V_O = 1.8$ V	92.8	
			$V_O = 3.3$ V	94.8	
		max I_O	$V_O = 0.6$ V	79.3	%
			$V_O = 1.0$ V	86.0	
			$V_O = 1.8$ V	90.7	
			$V_O = 3.3$ V	93.6	
P_d	Power dissipation at max I_O		$V_O = 0.6$ V	3.12	W
			$V_O = 1.0$ V	3.25	
			$V_O = 1.8$ V	3.68	
			$V_O = 3.3$ V	4.52	
P_{fi}	Input idling power (no load)	Default configuration: Continues Conduction Mode, CCM	$V_O = 0.6$ V	0.56	W
			$V_O = 1.0$ V	0.57	
			$V_O = 1.8$ V	0.68	
			$V_O = 3.3$ V	0.99	
P_{CTRL}	Input standby power	Turned off with CTRL-pin	Default configuration: Monitoring enabled, Precise timing enabled	180	mW

Technical Specification

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Characteristics		Conditions	min	typ	max	Unit
C_i	Internal input capacitance			70		μF
C_o	Internal output capacitance			200		μF
C_{OUT}	Total external output capacitance	See Note 10	300		15 000	μF
	ESR range of capacitors (per single capacitor)	See Note 10	5		30	$\text{m}\Omega$

V_{tr1}	Load transient peak voltage deviation Load step 25-75-25% of max I_o	Default configuration $di/dt = 2 \text{ A}/\mu\text{s}$ $C_o=470 \mu\text{F}$ (minimum external capacitance) see Note 13	$V_o = 0.6 \text{ V}$	85	mV
			$V_o = 1.0 \text{ V}$	85	
			$V_o = 1.8 \text{ V}$	90	
			$V_o = 3.3 \text{ V}$	135	
t_{tr1}	Load transient recovery time, Note 5 Load step 25-75-25% of max I_o	Default configuration $di/dt = 2 \text{ A}/\mu\text{s}$ $C_o=470 \mu\text{F}$ (minimum external capacitance) see Note 13	$V_o = 0.6 \text{ V}$	80	μs
			$V_o = 1.0 \text{ V}$	90	
			$V_o = 1.8 \text{ V}$	100	
			$V_o = 3.3 \text{ V}$	100	

f_s	Switching frequency		320	kHz
	Switching frequency range	PMBus configurable	200-640	kHz
	Switching frequency set-point accuracy		-5	5
	Control Circuit PWM Duty Cycle		5	95
	Minimum Sync Pulse Width		150	ns
	Synchronization Frequency Tolerance	External clock source	-13	13

Input Under Voltage Lockout, UVLO	UVLO threshold		3.85	V
	UVLO threshold range	PMBus configurable	3.85-14	V
	Set point accuracy		-150	150
	UVLO hysteresis		0.35	V
	UVLO hysteresis range	PMBus configurable	0-10.15	V
	Delay		2.5	μs
	Fault response	See Note 3	Automatic restart, 70ms	
Input Over Voltage Protection, IOVP	IOVP threshold		16	V
	IOVP threshold range	PMBus configurable	4.2-16	V
	Set point accuracy		-150	150
	IOVP hysteresis		1	V
	IOVP hysteresis range	PMBus configurable	0-11.8	V
	Delay		2.5	μs
	Fault response	See Note 3	Automatic restart, 70ms	
Power Good, PG, See Note 2	PG threshold		90	% V_o
	PG hysteresis		5	% V_o
	PG delay		10	ms
	PG delay range	PMBus configurable	0-500	s
Output voltage Over/Under Voltage Protection, OVP/UVP	UVP threshold		85	% V_o
	UVP threshold range	PMBus configurable	0-100	% V_o
	UVP hysteresis		5	% V_o
	OVP threshold		115	% V_o
	OVP threshold range	PMBus configurable	100-115	% V_o
	UVP/OVP response time		25	μs
	UVP/OVP response time range	PMBus configurable	5-60	μs
	Fault response	See Note 3	Automatic restart, 70ms	
Over Current Protection, OCP	OCP threshold		26	A
	OCP threshold range	PMBus configurable	0-26	A
	Protection delay, See Note 4		5	T_{sw}
	Protection delay range	PMBus configurable	1-32	T_{sw}
	Fault response	See Note 3	Automatic restart, 70ms	

Technical Specification

BMR 463 series POL Regulators Input 4.5-14 V, Output up to 20 A / 66 W

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Characteristics	Conditions	min	typ	max	Unit
Over Temperature Protection, OTP at P1 See Note 9	OTP threshold		120		°C
	OTP threshold range	PMBus configurable	-40...+120		°C
	OTP hysteresis		15		°C
	OTP hysteresis range	PMBus configurable	0-160		°C
	Fault response	See Note 3	Automatic restart, 70ms		

V _{IL}	Logic input low threshold	SYNC, SA0, SA1, SCL, SDA, GCB, CTRL, VSET		0.8	V
V _{IH}	Logic input high threshold		2		V
I _{IL}	Logic input low sink current	CTRL		0.6	mA
V _{OL}	Logic output low signal level			0.4	V
V _{OH}	Logic output high signal level	SYNC, SCL, SDA, SALERT, GCB, PG	2.25		V
I _{OL}	Logic output low sink current			4	mA
I _{OH}	Logic output high source current			2	mA
t _{set}	Setup time, SMBus	See Note 1	300		ns
t _{hold}	Hold time, SMBus	See Note 1	250		ns
t _{free}	Bus free time, SMBus	See Note 1	2		ms
C _p	Internal capacitance on logic pins			10	pF

Start-Up time		See Note 11	30		ms
Output Voltage Delay Time See Note 6	Delay duration		10		ms
	Delay duration range	PMBus configurable	2-500000		
	Delay accuracy	Default configuration: CTRL controlled Precise timing enabled	±0.25		ms
		PMBus controlled Precise timing disabled	-0.25/+4		ms
Output Voltage Ramp Time	Ramp duration		10		ms
	Ramp duration range	PMBus configurable	0-200		
	Ramp time accuracy		100		µs

VTRK Input Bias Current	V _{VTRK} = 5.5 V		110	200	µA
VTRK Tracking Ramp Accuracy, Note 8	100% Tracking (V _O - V _{VTRK})	-100		100	mV
VTRK Regulation Accuracy	100% Tracking (V _O - V _{VTRK})	-1		1	%

Max current difference between products in a sharing group			20		% of full scale
Number of products in a current sharing group				7	

Monitoring accuracy	READ_VIN vs V _I		3		%
	READ_VOUT vs V _O		1		%
	READ_IOUT vs I _O	I _O = 0-20 A, T _{P1} = 0 to +95°C V _I = 12 V	±1.4		A
	READ_IOUT vs I _O	I _O = 0-20 A, T _{P1} = 0 to +95°C V _I = 4.5-14 V	±2.6		A

Note 1: See section I2C/SMBus Setup and Hold Times – Definitions.

Note 2: Monitorable over PMBus Interface.

Note 3: Continuous re-starts with 70 ms between each start. See Power Management section for additional fault response types.

Note 4: T_{sw} is the switching period.

Note 5: Within +/-3% of V_O

Note 6: See section Soft-start Power Up.

Note 8: Tracking functionality is designed to follow a VTRK signal with slewrates < 2.4V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.

Note 9: See section Over Temperature Protection (OTP).

Note 10: See section External Capacitors.

Note 11: See section Start-Up Procedure.

Note 12: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.

Note 13: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.

BMR 463 series POL Regulators
Input 4.5-14 V, Output up to 20 A / 66 W

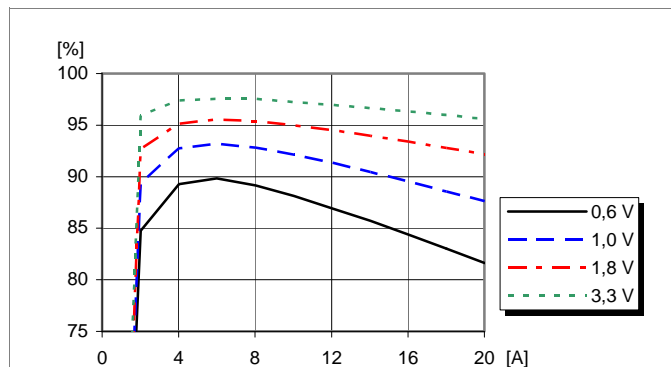
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Typical Characteristics Efficiency and Power Dissipation

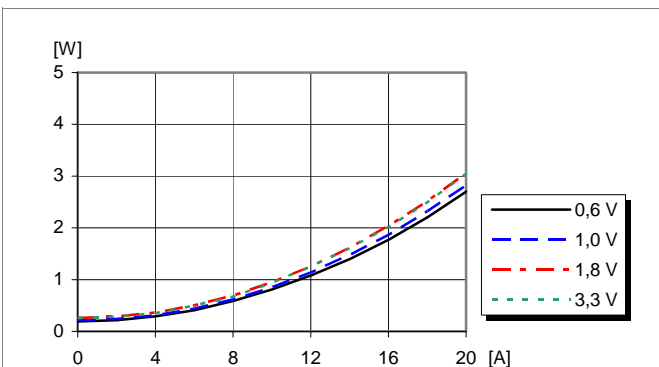
BMR 463 0002, BMR 463 1002

Efficiency vs. Output Current, $V_I=5\text{ V}$



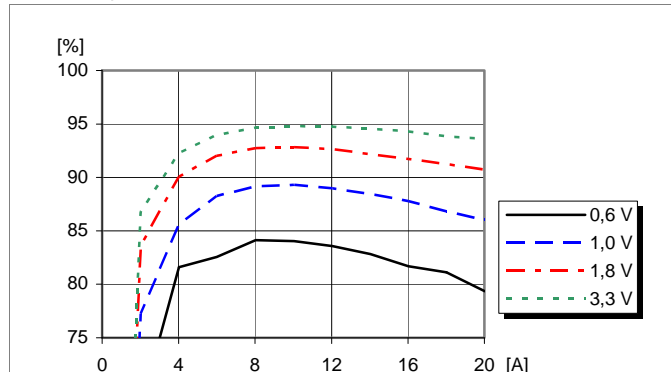
Efficiency vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=5\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Power Dissipation vs. Output Current, $V_I=5\text{ V}$



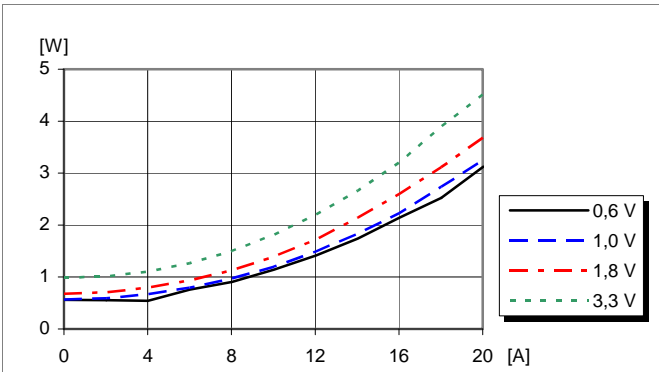
Dissipated power vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=5\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Efficiency vs. Output Current, $V_I=12\text{ V}$



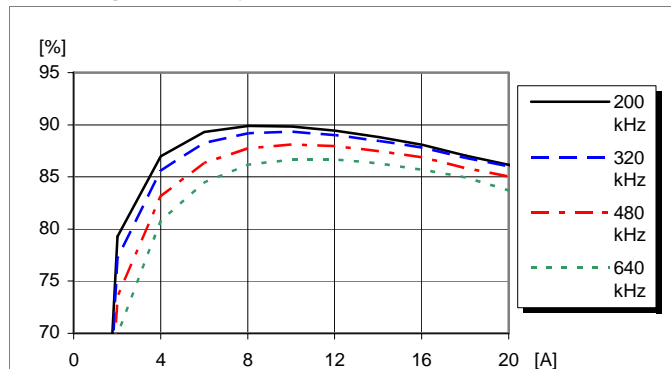
Efficiency vs. load current and output voltage at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Power Dissipation vs. Output Current, $V_I=12\text{ V}$



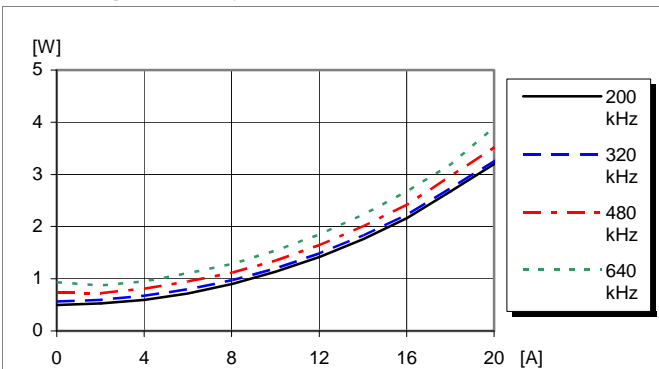
Dissipated power vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Efficiency vs. Output Current and Switching Frequency



Efficiency vs. load current and switch frequency at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $V_O=1.0\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
Default configuration except changed frequency

Power Dissipation vs. Output Current and Switching frequency



Dissipated power vs. load current and switch frequency at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $V_O=1.0\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
Default configuration except changed frequency

BMR 463 series POL Regulators
Input 4.5-14 V, Output up to 20 A / 66 W

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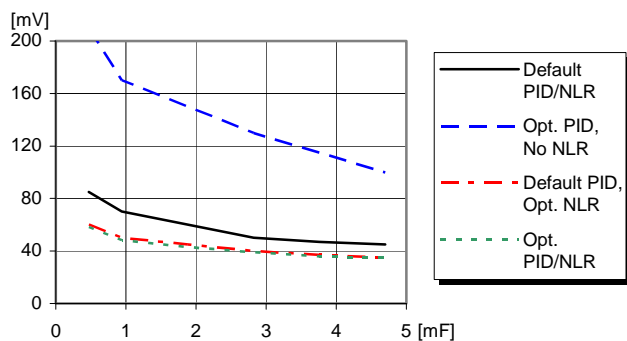
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Typical Characteristics

Load Transient

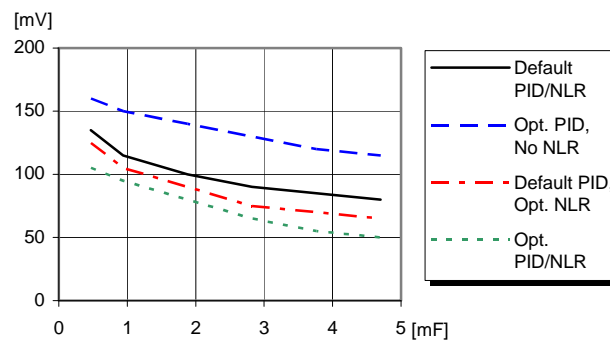
BMR 463 0002, BMR 463 1002

Load Transient vs. External Capacitance, $V_O=1.0$ V



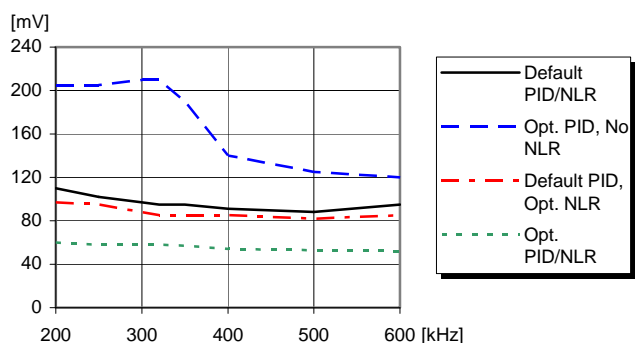
Load transient peak voltage deviation vs. external capacitance.
Step-change (5-15-5 A). Parallel coupling of capacitors with 470 μ F/10 m Ω ,
 $T_{P1} = +25^\circ\text{C}$. $V_I=12$ V, $V_O=1.0$ V, $f_{sw}=320$ kHz, $di/dt=2$ A/ μ s

Load Transient vs. External Capacitance, $V_O=3.3$ V



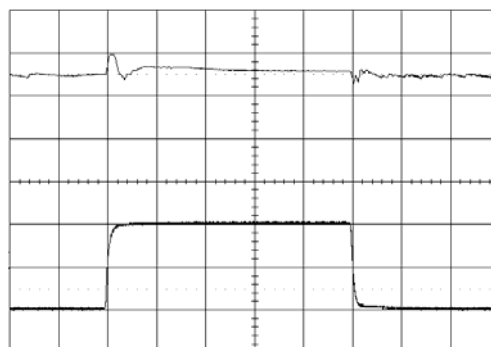
Load transient peak voltage deviation vs. external capacitance.
Step-change (5-15-5 A). Parallel coupling of capacitors with 470 μ F/10 m Ω ,
 $T_{P1} = +25^\circ\text{C}$. $V_I=12$ V, $V_O=3.3$ V, $f_{sw}=320$ kHz, $di/dt=2$ A/ μ s

Load transient vs. Switch Frequency



Load transient peak voltage deviation vs. frequency.
Step-change (5-15-5 A).
 $T_{P1} = +25^\circ\text{C}$. $V_I=12$ V, $V_O=1.0$ V, $C_O=470$ μ F/10 m Ω

Output Load Transient Response, Default PID/NLR



Output voltage response to load current step-change (5-15-5 A) at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12$ V, $V_O = 1.0$ V
 $di/dt=2$ A/ μ s, $f_{sw}=320$ kHz, $C_O=470$ μ F/10 m Ω

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

BMR 463 series POL Regulators
Input 4.5-14 V, Output up to 20 A / 66 W

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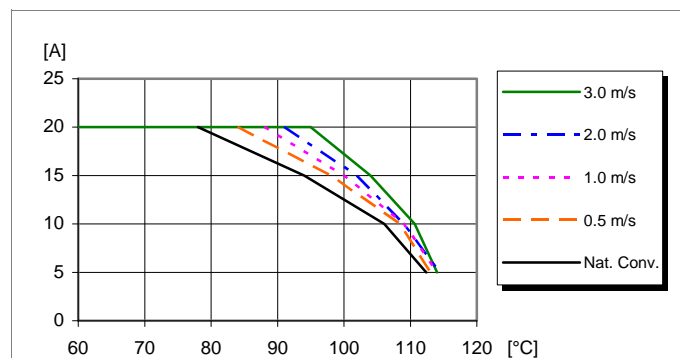
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Typical Characteristics

Output Current Characteristic

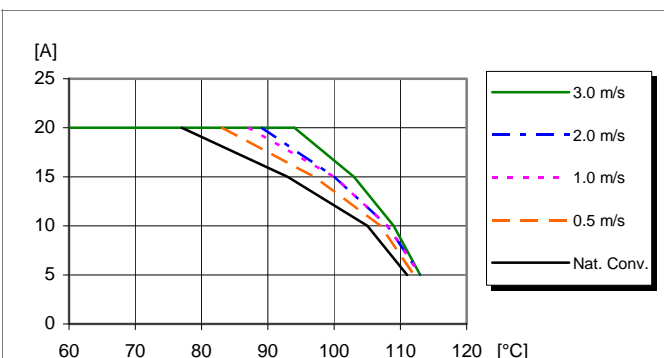
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Output Current Derating, $V_O=0.6$ V



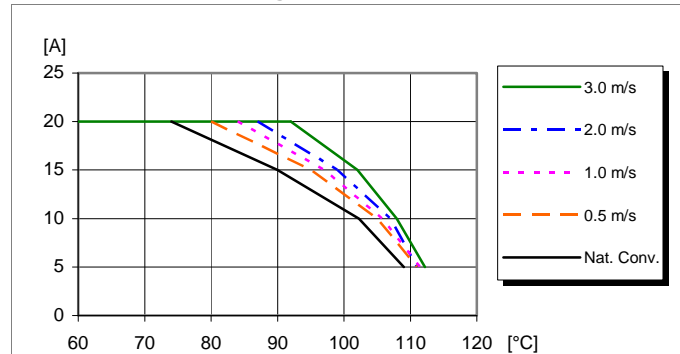
Available load current vs. ambient air temperature and airflow at $V_O=0.6$ V, $V_I=12$ V. See Thermal Consideration section.

Output Current Derating, $V_O=1.0$ V



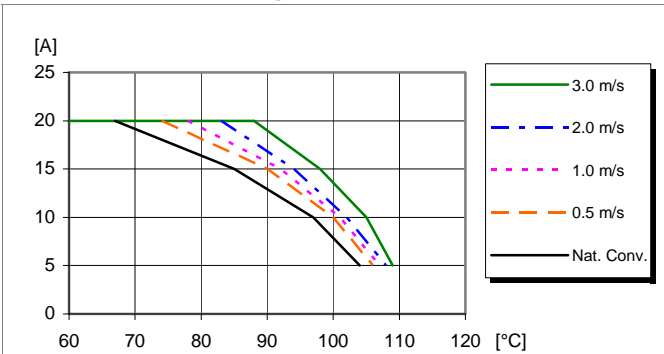
Available load current vs. ambient air temperature and airflow at $V_O=1.0$ V, $V_I=12$ V. See Thermal Consideration section.

Output Current Derating, $V_O=1.8$ V



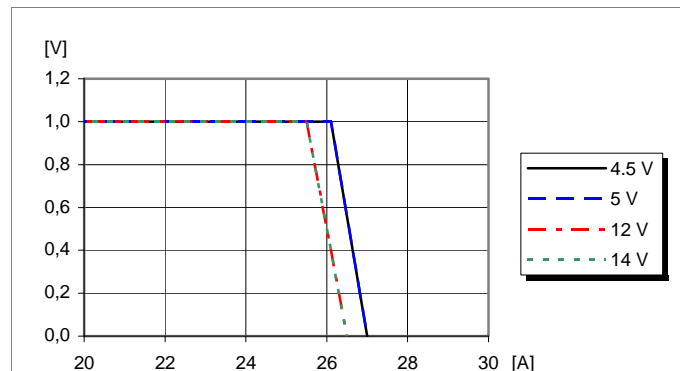
Available load current vs. ambient air temperature and airflow at $V_O=1.8$ V, $V_I=12$ V. See Thermal Consideration section.

Output Current Derating, $V_O=3.3$ V



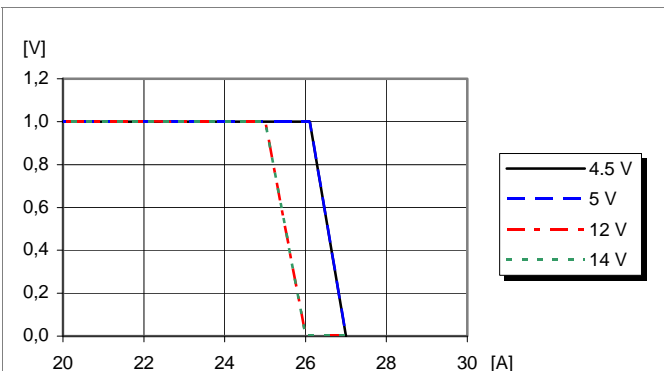
Available load current vs. ambient air temperature and airflow at $V_O=3.3$ V, $V_I=12$ V. See Thermal Consideration section.

Current Limit Characteristics, $V_O=1.0$ V



Output voltage vs. load current at $T_{P1} = +25^\circ\text{C}$. $V_O=1.0$ V.

Current Limit Characteristics, $V_O=3.3$ V



Output voltage vs. load current at $T_{P1} = +25^\circ\text{C}$. $V_O=3.3$ V.

BMR 463 series POL Regulators
Input 4.5-14 V, Output up to 20 A / 66 W

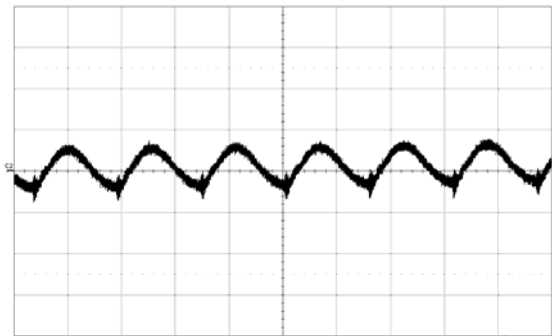
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Typical Characteristics Output Voltage

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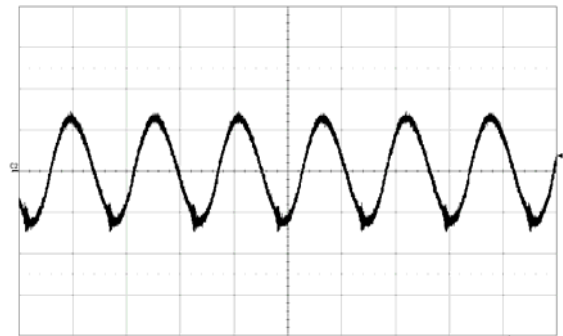
Output Ripple & Noise, $V_O=1.0\text{ V}$



Output voltage ripple at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
 $I_O = 20\text{ A}$

Trace: output voltage (20 mV/div.).
Time scale: (2 $\mu\text{s}/\text{div.}$).

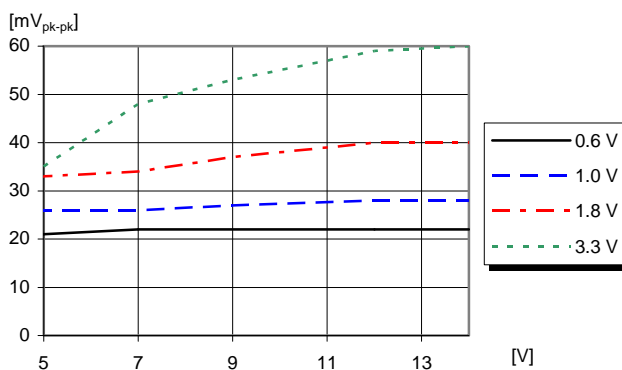
Output Ripple & Noise, $V_O=3.3\text{ V}$



Output voltage ripple at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
 $I_O = 20\text{ A}$

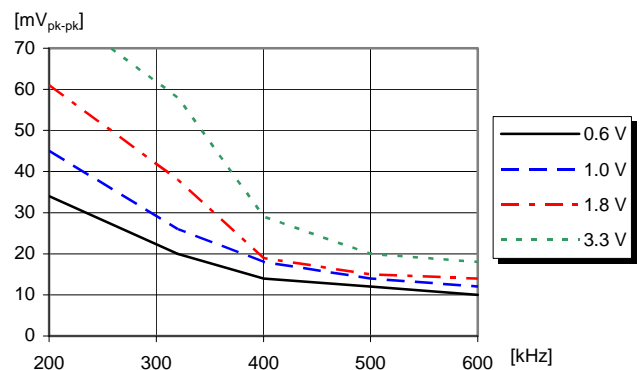
Trace: output voltage (20 mV/div.).
Time scale: (2 $\mu\text{s}/\text{div.}$).

Output Ripple vs. Input Voltage



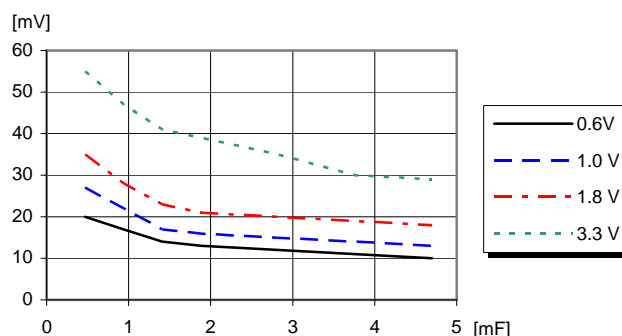
Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$,
 $I_O = 20\text{ A}$

Output Ripple vs. Frequency



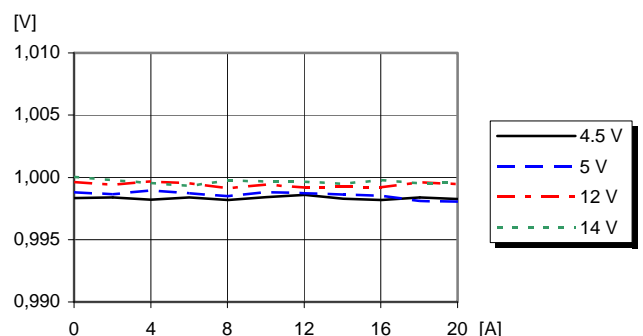
Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$,
 $I_O = 20\text{ A}$. Default configuration except changed frequency.

Output Ripple vs. External Capacitance



Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $I_O = 20\text{ A}$. Parallel coupling
of capacitors with $470\text{ }\mu\text{F}/10\text{ m}\Omega$,

Load regulation, $V_O=1.0\text{ V}$



Load regulation at $V_O=1.0\text{ V}$ at: $T_{P1} = +25^\circ\text{C}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$

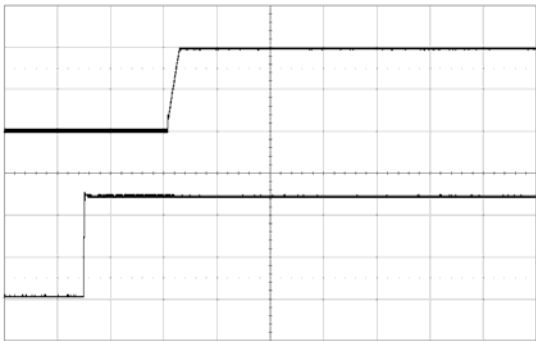
BMR 463 series POL Regulators
Input 4.5-14 V, Output up to 20 A / 66 W

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Typical Characteristics
Start-up and shut-down

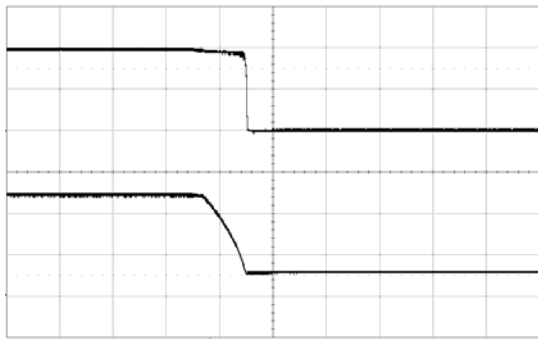
BMR 463 0002, BMR 463 1002

Start-up by input source



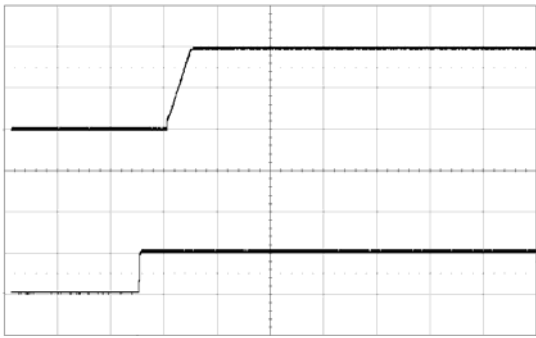
Start-up enabled by connecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 1.0\text{ V}$
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 20\text{ A}$
Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (20 ms/div.).

Shut-down by input source



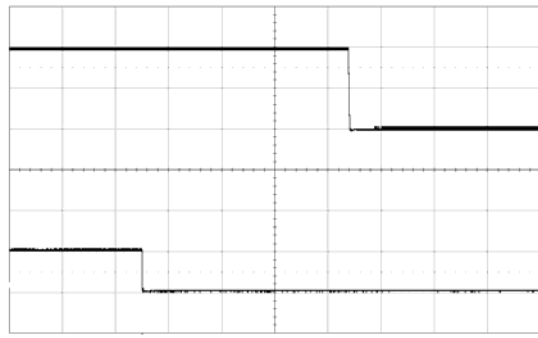
Shut-down enabled by disconnecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 1.0\text{ V}$
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 20\text{ A}$
Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (2 ms/div.).

Start-up by CTRL signal



Start-up by enabling CTRL signal at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 1.0\text{ V}$
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 20\text{ A}$
Top trace: output voltage (0.5 V/div.).
Bottom trace: CTRL signal (5 V/div.).
Time scale: (20 ms/div.).

Shut-down by CTRL signal



Shut-down enabled by disconnecting V_I at:
 $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12\text{ V}$, $V_O = 1.0\text{ V}$
 $C_O = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 20\text{ A}$
Top trace: output voltage (0.5 V/div.).
Bottom trace: CTRL signal (5 V/div.).
Time scale: (2 ms/div.).

BMR 463 series POL Regulators
Input 4.5-14 V, Output up to 20 A / 66 W

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Electrical Specification
BMR 463 2002 (SIP)
 $T_{P1} = -30$ to $+95^{\circ}\text{C}$, $V_I = 4.5$ to 14 V , $V_I > V_O + 1.0\text{ V}$

Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_I = 12.0\text{ V}$, max I_O , unless otherwise specified under Conditions.

Default configuration file, 190 10-CDA 102 0258/001.

External $C_{IN} = 470\text{ }\mu\text{F}/10\text{ m}\Omega$, $C_{OUT} = 470\text{ }\mu\text{F}/10\text{ m}\Omega$. See Operating Information section for selection of capacitor types.

Sense pins are connected to the output pins.

Characteristics	Conditions	min	typ	max	Unit
V_I	Input voltage rise time			2.4	V/ms

V_O	Output voltage without pin strap		1.2		V
	Output voltage adjustment range	0.60		3.3	V
	Output voltage adjustment including margining	0.54		3.63	V
	Output voltage set-point resolution		± 0.025		% V_O
	Output voltage accuracy	Includes, line, load, temp.	-1	1	%
	Line regulation	$V_O = 0.6\text{ V}$	2		mV
		$V_O = 1.0\text{ V}$	2		
		$V_O = 1.8\text{ V}$	3		
		$V_O = 3.3\text{ V}$	3		
	Load regulation; $I_O = 0 - 100\%$	$V_O = 0.6\text{ V}$	3		mV
		$V_O = 1.0\text{ V}$	2		
		$V_O = 1.8\text{ V}$	2		
		$V_O = 3.3\text{ V}$	2		
V_{Oac}	Output ripple & noise $C_O = 470\text{ }\mu\text{F}$ (minimum external capacitance). See Note 12	$V_O = 0.6\text{ V}$	20		mVp-p
		$V_O = 1.0\text{ V}$	30		
		$V_O = 1.8\text{ V}$	40		
		$V_O = 3.3\text{ V}$	60		

I_O	Output current		20		A
I_S	Static input current at max I_O	$V_O = 0.6\text{ V}$	1.29		A
		$V_O = 1.0\text{ V}$	1.97		
		$V_O = 1.8\text{ V}$	3.34		
		$V_O = 3.3\text{ V}$	5.92		
I_{lim}	Current limit threshold		22	30	A
I_{sc}	Short circuit current	RMS, hiccup mode, See Note 3	$V_O = 0.6\text{ V}$	8	A
			$V_O = 1.0\text{ V}$	6	
			$V_O = 1.8\text{ V}$	5	
			$V_O = 3.3\text{ V}$	4	

η	Efficiency	50% of max I_O	$V_O = 0.6\text{ V}$	83.5	%
			$V_O = 1.0\text{ V}$	89.0	
			$V_O = 1.8\text{V}$	92.7	
			$V_O = 3.3\text{ V}$	94.8	
		max I_O	$V_O = 0.6\text{ V}$	78.0	%
			$V_O = 1.0\text{ V}$	85.3	
			$V_O = 1.8\text{V}$	90.4	
			$V_O = 3.3\text{ V}$	93.5	
P_d	Power dissipation at max I_O	$V_O = 0.6\text{ V}$	3.40	W	
		$V_O = 1.0\text{ V}$	3.45		
		$V_O = 1.8\text{V}$	3.86		
		$V_O = 3.3\text{ V}$	4.62		
P_{ii}	Input idling power (no load)	Default configuration: Continues Conduction Mode, CCM	$V_O = 0.6\text{ V}$	0.56	W
			$V_O = 1.0\text{ V}$	0.57	
			$V_O = 1.8\text{V}$	0.69	
			$V_O = 3.3\text{ V}$	1.00	
P_{CTRL}	Input standby power	Turned off with CTRL-pin	Default configuration: Monitoring enabled, Precise timing enabled	180	mW

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Characteristics		Conditions	min	typ	max	Unit
C_i	Internal input capacitance			70		μF
C_o	Internal output capacitance			200		μF
C_{OUT}	Total external output capacitance	See Note 10	300		15 000	μF
	ESR range of capacitors (per single capacitor)	See Note 10	5		30	m Ω

V_{tr1}	Load transient peak voltage deviation	Default configuration $di/dt = 2 \text{ A}/\mu\text{s}$ $C_o=470 \mu\text{F}$ (minimum external capacitance) see Note 13	$V_o = 0.6 \text{ V}$	75	mV
			$V_o = 1.0 \text{ V}$	80	
			$V_o = 1.8 \text{ V}$	105	
			$V_o = 3.3 \text{ V}$	120	
t_{tr1}	Load transient recovery time, Note 5	Default configuration $di/dt = 2 \text{ A}/\mu\text{s}$ $C_o=470 \mu\text{F}$ (minimum external capacitance) see Note 13	$V_o = 0.6 \text{ V}$	40	μs
			$V_o = 1.0 \text{ V}$	50	
			$V_o = 1.8 \text{ V}$	100	
			$V_o = 3.3 \text{ V}$	100	

f _s	Switching frequency		320	kHz	
	Switching frequency range	PMBus configurable	200-640	kHz	
	Switching frequency set-point accuracy		-5	5	%
	Control Circuit PWM Duty Cycle		5	95	%
	Minimum Sync Pulse Width		150		ns
	Synchronization Frequency Tolerance	External clock source	-13	13	%

Input Under Voltage Lockout, UVLO	UVLO threshold		3.85	V
	UVLO threshold range	PMBus configurable	3.85-14	V
	Set point accuracy		-150150	mV
	UVLO hysteresis		0.35	V
	UVLO hysteresis range	PMBus configurable	0-10.15	V
	Delay		2.5	μs
	Fault response	See Note 3	Automatic restart, 70ms	
Input Over Voltage Protection, IOVP	IOVP threshold		16	V
	IOVP threshold range	PMBus configurable	4.2-16	V
	Set point accuracy		-150150	mV
	IOVP hysteresis		1	V
	IOVP hysteresis range	PMBus configurable	0-11.8	V
	Delay		2.5	μs
	Fault response	See Note 3	Automatic restart, 70ms	
Power Good, PG, See Note 2	PG threshold		90	% V _O
	PG hysteresis		5	% V _O
	PG delay		10	ms
	PG delay range	PMBus configurable	0-500	s
Output voltage Over/Under Voltage Protection, OVP/UVP	UVP threshold		85	% V _O
	UVP threshold range	PMBus configurable	0-100	% V _O
	UVP hysteresis		5	% V _O
	OVP threshold		115	% V _O
	OVP threshold range	PMBus configurable	100-115	% V _O
	UVP/OVP response time		25	μs
	UVP/OVP response time range	PMBus configurable	5-60	μs
	Fault response	See Note 3	Automatic restart, 70ms	
Over Current Protection, OCP	OCP threshold		26	A
	OCP threshold range	PMBus configurable	0-26	A
	Protection delay,	See Note 4	5	T _{sw}
	Protection delay range	PMBus configurable	1-32	T _{sw}
	Fault response	See Note 3	Automatic restart, 70ms	

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Characteristics	Conditions	min	typ	max	Unit
Over Temperature Protection, OTP at P1 See Note 9	OTP threshold		120		°C
	OTP threshold range	PMBus configurable	-40...+120		°C
	OTP hysteresis		15		°C
	OTP hysteresis range	PMBus configurable	0-160		°C
	Fault response	See Note 3	Automatic restart, 70ms		

V _{IL}	Logic input low threshold	SYNC, SA0, SA1, SCL, SDA, GCB, CTRL, VSET		0.8	V
V _{IH}	Logic input high threshold		2		V
I _{IL}	Logic input low sink current	CTRL		0.6	mA
V _{OL}	Logic output low signal level			0.4	V
V _{OH}	Logic output high signal level	SYNC, SCL, SDA, SALERT, GCB, PG	2.25		V
I _{OL}	Logic output low sink current			4	mA
I _{OH}	Logic output high source current			2	mA
t _{set}	Setup time, SMBus	See Note 1	300		ns
t _{hold}	Hold time, SMBus	See Note 1	250		ns
t _{free}	Bus free time, SMBus	See Note 1	2		ms
C _p	Internal capacitance on logic pins			10	pF

Start-Up time		See Note 11	30		ms
Output Voltage Delay Time See Note 6	Delay duration		10		ms
	Delay duration range	PMBus configurable	2-500000		
	Delay accuracy	Default configuration: CTRL controlled	±0.25		ms
		PMBus controlled Precise timing enabled	-0.25/+4		ms
Output Voltage Ramp Time	Ramp duration		10		ms
	Ramp duration range	PMBus configurable	0-200		
	Ramp time accuracy		100		µs

VTRK Input Bias Current	V _{VTRK} = 5.5 V		110	200	µA
VTRK Tracking Ramp Accuracy, Note 8	100% Tracking (V _O - V _{VTRK})	-100		100	mV
VTRK Regulation Accuracy	100% Tracking (V _O - V _{VTRK})	-1		1	%

Max current difference between products in a sharing group			20		% of full scale
Number of products in a current sharing group				7	

Monitoring accuracy	READ_VIN vs V _I		3		%
	READ_VOUT vs V _O		1		%
	READ_IOUT vs I _O	I _O = 0-20 A, T _{P1} = 0 to +95°C V _I = 12 V	±1.4		A
	READ_IOUT vs I _O	I _O = 0-20 A, T _{P1} = 0 to +95°C V _I = 4.5-14 V	±2.6		A

Note 1: See section I2C/SMBus Setup and Hold Times – Definitions.

Note 2: Monitorable over PMBus Interface.

Note 3: Continuous re-starts with 70 ms between each start. See Power Management section for additional fault response types.

Note 4: T_{sw} is the switching period.Note 5: Within +/-3% of V_O.

Note 6: See section Soft-start Power Up.

Note 8: Tracking functionality is designed to follow a VTRK signal with slewrates < 2.4V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.

Note 9: See section Over Temperature Protection (OTP).

Note 10: See section External Capacitors.

Note 11: See section Start-Up Procedure.

Note 12: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.

Note 13: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.

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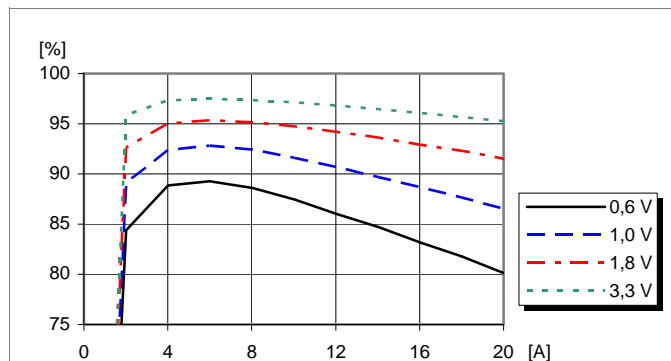
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Typical Characteristics Efficiency and Power Dissipation

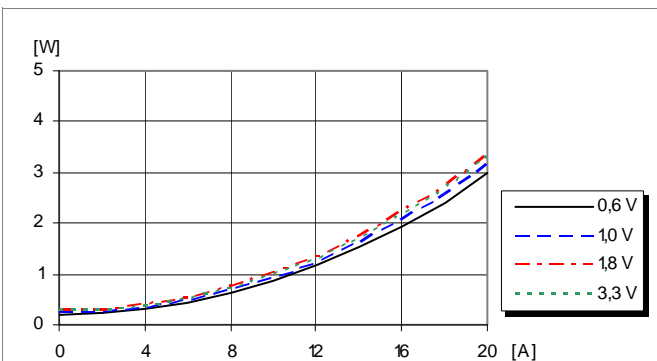
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Efficiency vs. Output Current, $V_I=5\text{ V}$



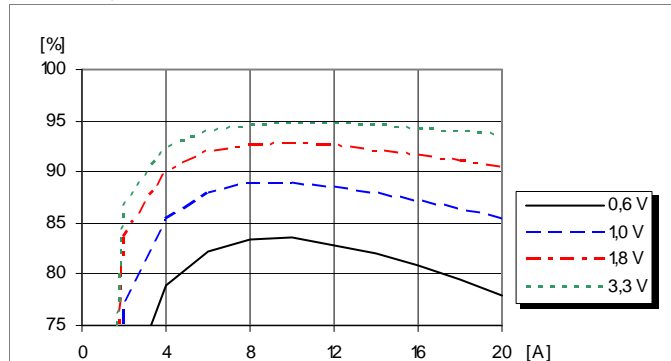
Efficiency vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=5\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Power Dissipation vs. Output Current, $V_I=5\text{ V}$



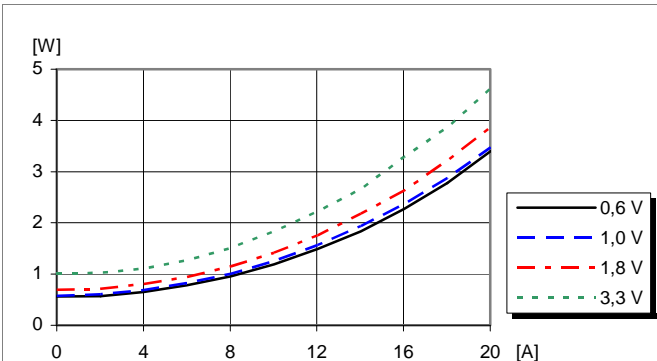
Dissipated power vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=5\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Efficiency vs. Output Current, $V_I=12\text{ V}$



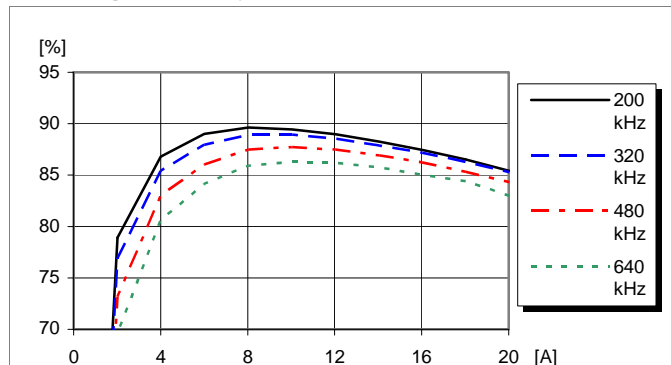
Efficiency vs. load current and output voltage at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Power Dissipation vs. Output Current, $V_I=12\text{ V}$



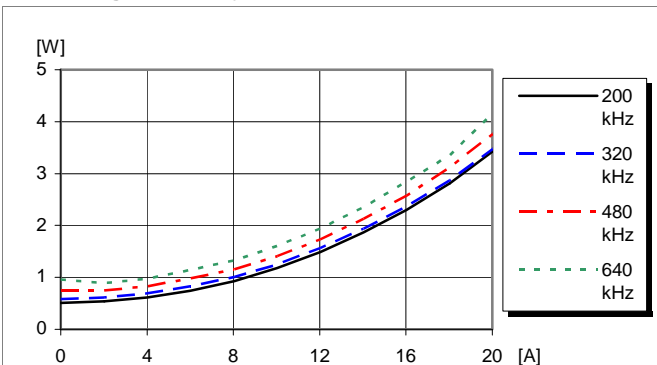
Dissipated power vs. load current and output voltage:
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Efficiency vs. Output Current and Switching Frequency



Efficiency vs. load current and switch frequency at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $V_O=1.0\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
Default configuration except changed frequency

Power Dissipation vs. Output Current and Switching frequency



Dissipated power vs. load current and switch frequency at
 $T_{P1} = +25^\circ\text{C}$, $V_I=12\text{ V}$, $V_O=1.0\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
Default configuration except changed frequency

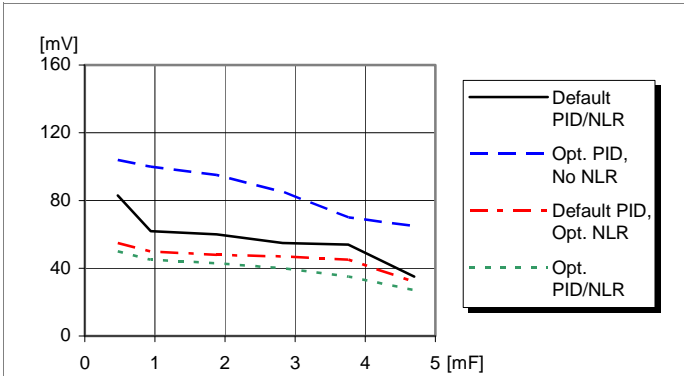
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Typical Characteristics
Load Transient

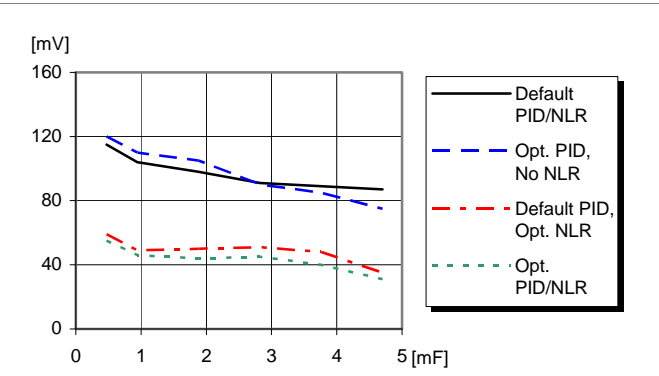
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Load Transient vs. External Capacitance, $V_O=1.0\text{ V}$



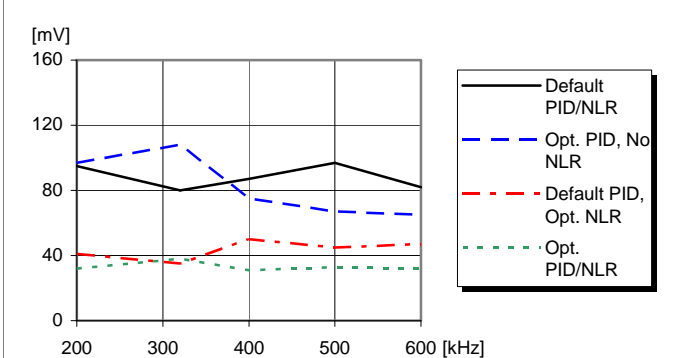
Load transient peak voltage deviation vs. external capacitance.
Step-change (5-15-5 A). Parallel coupling of capacitors with 470 $\mu\text{F}/10\text{ m}\Omega$,
 $T_{P1} = +25^\circ\text{C}$. $V_I=12\text{ V}$, $V_O=1.0\text{ V}$, $f_{sw}=320\text{ kHz}$, $di/dt=2\text{ A}/\mu\text{s}$

Load Transient vs. External Capacitance, $V_O=3.3\text{ V}$



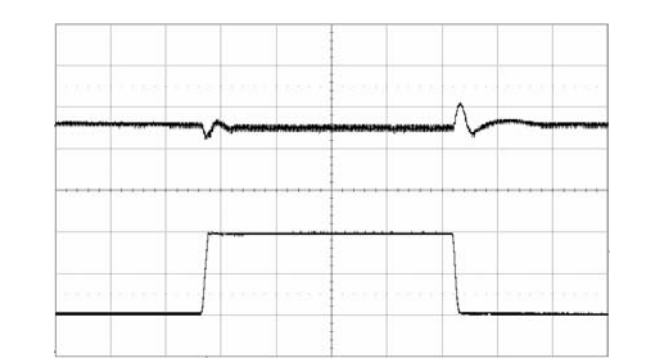
Load transient peak voltage deviation vs. external capacitance.
Step-change (5-15-5 A). Parallel coupling of capacitors with 470 $\mu\text{F}/10\text{ m}\Omega$,
 $T_{P1} = +25^\circ\text{C}$. $V_I=12\text{ V}$, $V_O=3.3\text{ V}$, $f_{sw}=320\text{ kHz}$, $di/dt=2\text{ A}/\mu\text{s}$

Load transient vs. Switch Frequency



Load transient peak voltage deviation vs. frequency.
Step-change (5-15-5 A).
 $T_{P1} = +25^\circ\text{C}$. $V_I=12\text{ V}$, $V_O=1.0\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$

Output Load Transient Response, Default PID/NLR



Output voltage response to load current step-change (5-15-5 A) at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $V_O = 1.0\text{ V}$
 $di/dt=2\text{ A}/\mu\text{s}$, $f_{sw}=320\text{ kHz}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

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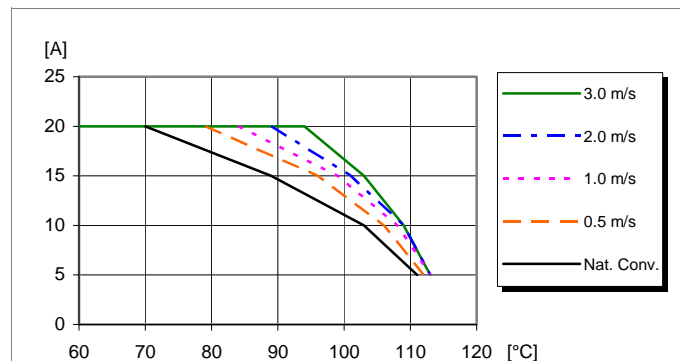
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Typical Characteristics

Output Current Characteristic

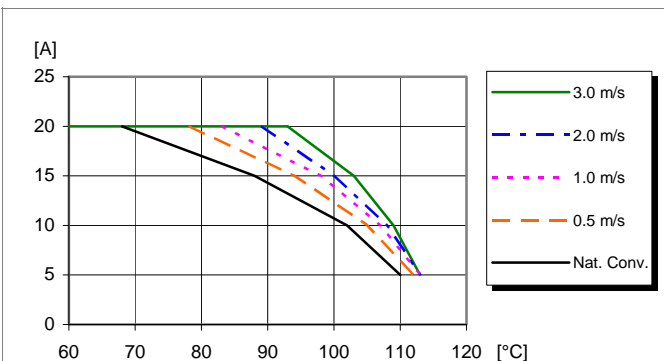
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Output Current Derating, $V_O=0.6\text{ V}$



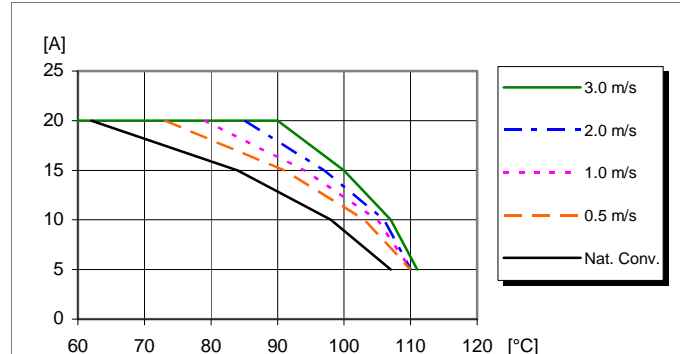
Available load current vs. ambient air temperature and airflow at $V_O=0.6\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Output Current Derating, $V_O=1.0\text{ V}$



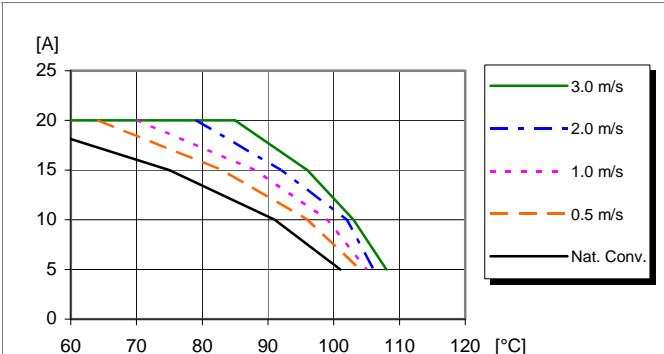
Available load current vs. ambient air temperature and airflow at $V_O=1.0\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Output Current Derating, $V_O=1.8\text{ V}$



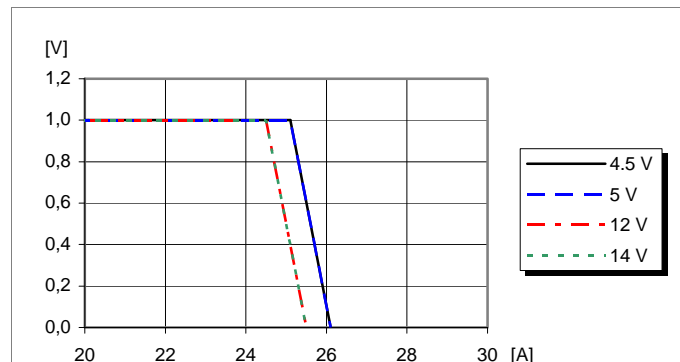
Available load current vs. ambient air temperature and airflow at $V_O=1.8\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Output Current Derating, $V_O=3.3\text{ V}$



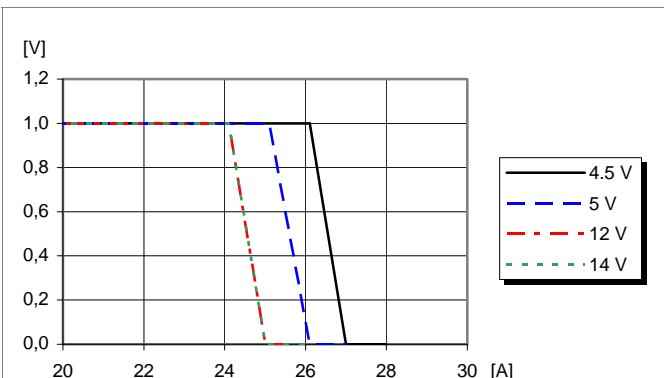
Available load current vs. ambient air temperature and airflow at $V_O=3.3\text{ V}$, $V_I=12\text{ V}$. See Thermal Consideration section.

Current Limit Characteristics, $V_O=1.0\text{ V}$



Output voltage vs. load current at $T_{P1} = +25^\circ\text{C}$. $V_O=1.0\text{ V}$.

Current Limit Characteristics, $V_O=3.3\text{ V}$



Output voltage vs. load current at $T_{P1} = +25^\circ\text{C}$. $V_O=3.3\text{ V}$.

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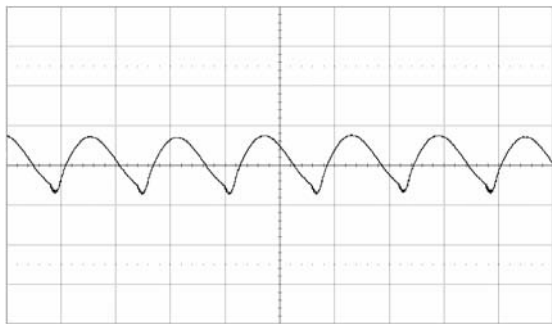
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Typical Characteristics

Output Voltage

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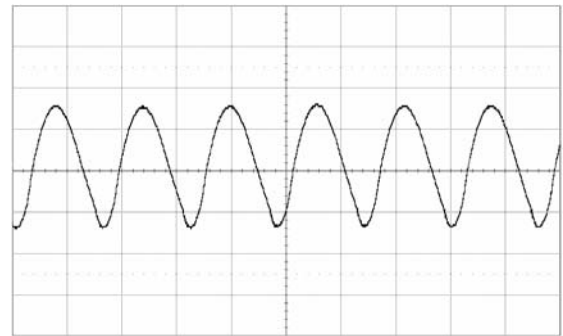
Output Ripple & Noise, $V_O=1.0\text{ V}$



Output voltage ripple at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
 $I_O = 20\text{ A}$

Trace: output voltage (10 mV/div.).
Time scale: (2 $\mu\text{s}/\text{div.}$).

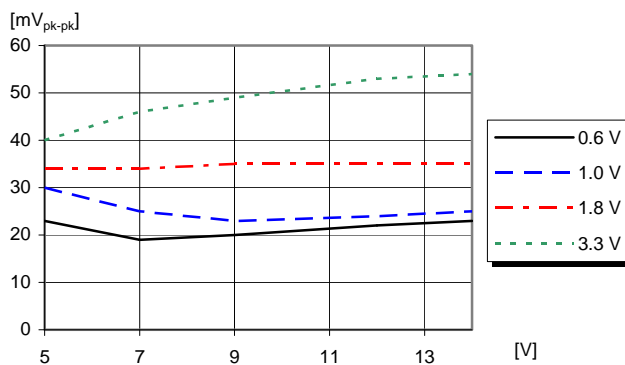
Output Ripple & Noise, $V_O=3.3\text{ V}$



Output voltage ripple at:
 $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$
 $I_O = 20\text{ A}$

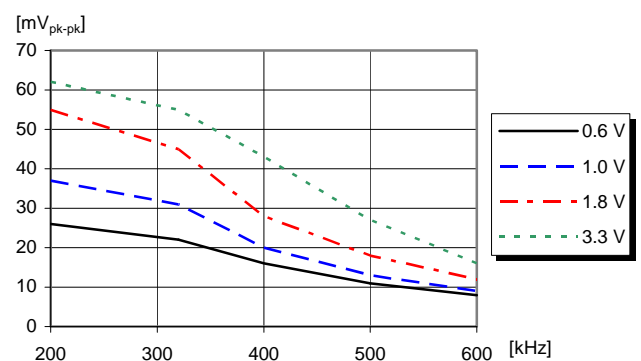
Trace: output voltage (10 mV/div.).
Time scale: (2 $\mu\text{s}/\text{div.}$).

Output Ripple vs. Input Voltage



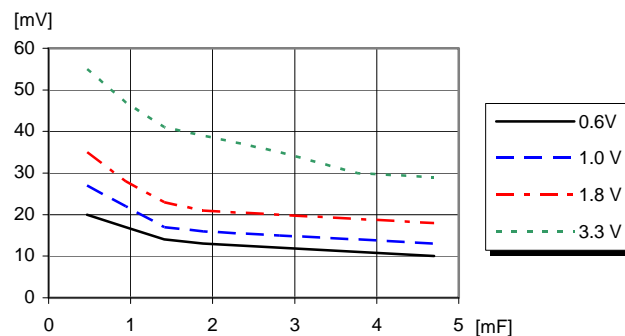
Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 20\text{ A}$.

Output Ripple vs. Frequency



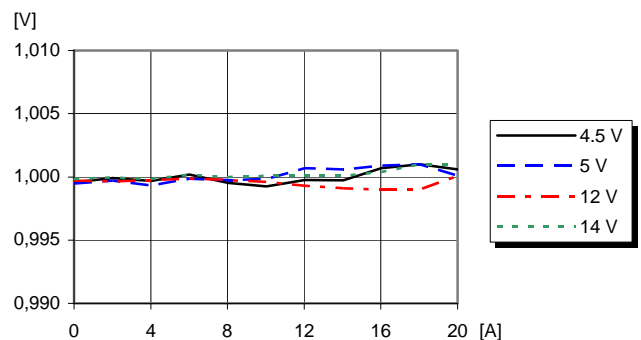
Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$, $I_O = 20\text{ A}$. Default configuration except changed frequency.

Output Ripple vs. External Capacitance



Output voltage ripple V_{pk-pk} at: $T_{P1} = +25^\circ\text{C}$, $V_I = 12\text{ V}$, $I_O = 20\text{ A}$. Parallel coupling of capacitors with $470\text{ }\mu\text{F}/10\text{ m}\Omega$.

Load regulation, $V_O=1.0\text{ V}$



Load regulation at $V_O=1.0\text{ V}$ at: $T_{P1} = +25^\circ\text{C}$, $C_O=470\text{ }\mu\text{F}/10\text{ m}\Omega$