Standby for a breakthrough in losses

Abstract

Energy-saving regulations demand that power converters dissipate minimum power at light load and in standby modes while achieving high efficiency under operating loads. Additionally, cost pressures require circuits to be ever simpler. These opposing demands are satisfied by using a SiC JFET die for the power switch in standby converters which results in high operating efficiency and which can be configured to generate a start-up auxiliary supply. This supply is naturally disconnected when the converter operates enabling low loss conversion.

Blog

What would you do with $19 billion? According to the Natural Resources Defense Council, that's what was paid in 2015 by US citizens in electricity bills for devices and appliances that were just in 'standby' mode [1]. OK your share is only $60 but there's an environmental cost as well, equivalent to the operation of fifty large power plants, so various initiatives and regulations are in place to minimise the effect such as those from Energy Star™ in the US and the Ecodesign directive in Europe. Typical acceptable standby loss is less than 0.5W but for a '5-star' rating it needs to be less than 30mW.

At the other end of the scale, full load losses in devices and appliances need to be low as well, not just for energy saving but for the knock-on benefit of smaller size for less heat dissipated. This means high conversion efficiency in the power conversion stage. Couple this with the relentless pressure for lower costs and AC-DC converter designers are faced with a tough challenge.

Latest technologies in high power converters using Wide-Band-Gap (WBG) semiconductors are yielding efficiencies in the high 90s and in standby, an effective solution for low dissipation is to disable the main converter completely and leave a small auxiliary converter running to keep the device ready for a quick start. This means that low power converters, typically fly-backs, define standby losses in large equipment as well as losses when they are a main power source such as for cell-phone chargers and small devices. When trying to maximise the efficiency of low power AC-DCs, every milliwatt of loss counts and a significant

contributor is the circuit that provides power for the control IC. Initially, start-up current must come from the AC mains so a high voltage, high-power dropper resistor, or several in series, is sometimes used with a zener diode which is often in the IC, to clamp the voltage. The resistor has to be sized to allow enough start-up current at low AC line but at high line the voltage dropped across the resistor might be 3x giving 9x dissipation with 3x current and dissipation in the zener.

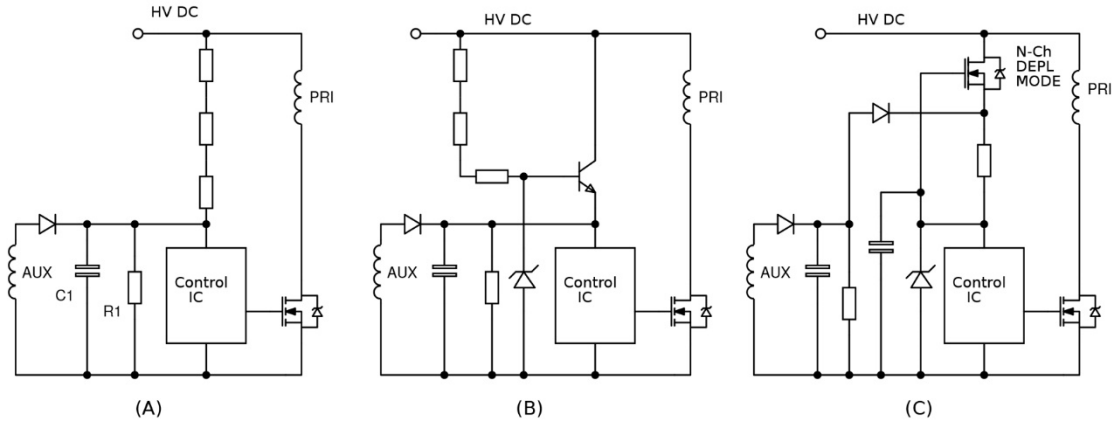

Figure 1: Traditional converter IC start-up schemes

You can quickly see watts of power lost under worst-case conditions so a solution is to make the resistor a very high value and let it charge a capacitor which then releases enough start-up energy when the IC undervoltage lockout is reached. An auxiliary supply then takes over. **(Figure 1a**). The auxiliary supply may need a pre-load (R1) to prevent the auxiliary supply exceeding the zener voltage under all operating conditions. To minimise dissipation, both resistor and capacitor have to be such high values though, that start-up time might be several seconds and unacceptable. A series transistor (Figure 1b), helps to move the dissipation from the zener in the IC but is just moving the problem. Extra complexity to switch the transistor off after the converter starts using the auxiliary supply is a solution but this adds costs and there is still dissipation in the biasing of the transistor. Another solution is to use a high voltage n-channel depletion mode MOSFET (Figure 1c). This needs no gate biasing from the high voltage but these components are relatively rare and expensive and still several additional parts are needed.

There is an innovative solution to the problem though which entails re-thinking the overall design but gives multiple benefits. Control ICs drive an external MOSFET which can be used

with a JFET in a cascode configuration (**Figure 2**). If a high voltage SIC JFET is used, it can switch dramatically fast with very low losses and is extremely robust with short circuits and overvoltages. The MOSFET in this configuration can be a low voltage type, typically 30V rating.

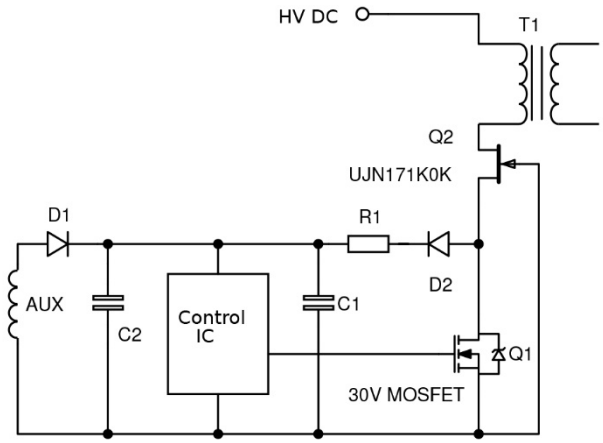

Figure 2: SiC JFET enables simple and efficient start-up

The magic comes when you examine the conditions at start-up – because the SiC JFET is normally-ON, it supplies current through D2 and R1 into C1 until the IC undervoltage lockout is reached and the circuit starts to switch. The source of the SiC JFET cannot exceed about 10V as this would cut-off the channel, with the SiC JFET gate at 0V, so R2 can be a relatively low value for a quick start up with little dissipation. D2 is a low-cost, low voltage diode. An auxiliary supply from a winding on the power transformer set for about 12V can then take over, reverse biasing D2 with no further dissipation in the start-up circuit.

The low voltage MOSFET is an extra component and low-cost but could be eliminated if it were on the die in the control IC. In fact, it might effectively be there already as the drive to the IC output transistor which then could be eliminated, saving cost again. A stage further is to co-package a SiC JFET die with the control IC die for a very compact and cost-effective solution. SiC JFET die from UnitedSiC [2] are an excellent choice for this approach with their high voltage ratings up to 1700V, low R_{DSON} down to 140 milliohms and die size down to 800 microns square. SiC has an inherent high temperature rating with thermal conductivity 3.5 x better than silicon so despite the small die size, it can transfer heat very effectively in typical IC packages.

References

[1] https://www.nrdc.org/sites/default/files/home-idle-load-IP.pdf

[2] UnitedSiC.com

END